



B460H6-M14

VER : A

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REVISION HISTORY:

Rev	Date	Notes
V.A	2020/01/06	Base on H410H6-M7 V1.0 change to B460H6-M14 VA.

Intel® 400 Series (CML PCH-V) Chipset HSIO Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
USB 3.2 Gen 1 x1	USB 3.2 Gen 1 x2	USB 3.2 Gen 1 x3	USB 3.2 Gen 1 x4	USB 3.2 Gen 1 x5	USB 3.2 Gen 1 x6	USB 3.2 Gen 1 x7	USB 3.2 Gen 1 x8	USB 3.2 Gen 1 x9	USB 3.2 Gen 1 x10	PCIe 10.0 x1	PCIe 10.0 x2	PCIe 10.0 x4	PCIe 10.0 x8	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	PCIe 10.0 x16	
1) SATA #0/#1 can be configured to PCIe* Ports 9/10 or 13/14.																													

SKU

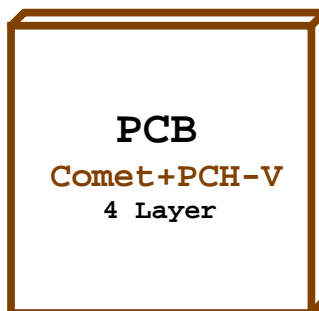
H410	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe LAN	PCIe	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B460	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	USB 3.2 Gen 1	PCIe	PCIe LAN	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe SATA	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe

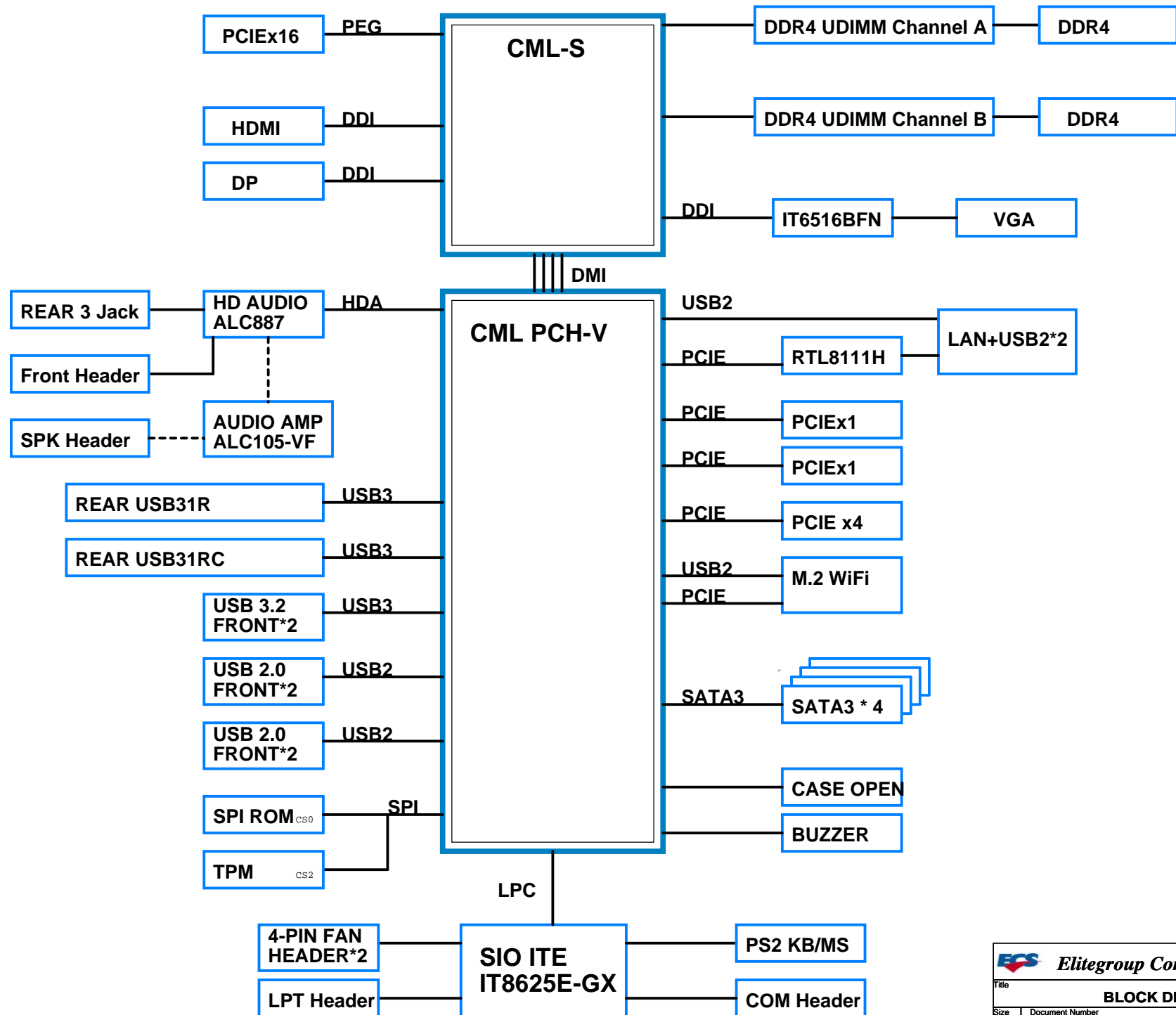
SKU	PCIe storage												1) SATA #0/1 can be configured to PCIe* Ports 9/10 or 13/14.																	
H410	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	N/A	N/A	N/A	N/A	LAN Only	PCIe LAN	PCIe LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B460	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	USB3.2 Gen 1	PCIe	PCIe LAN	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe

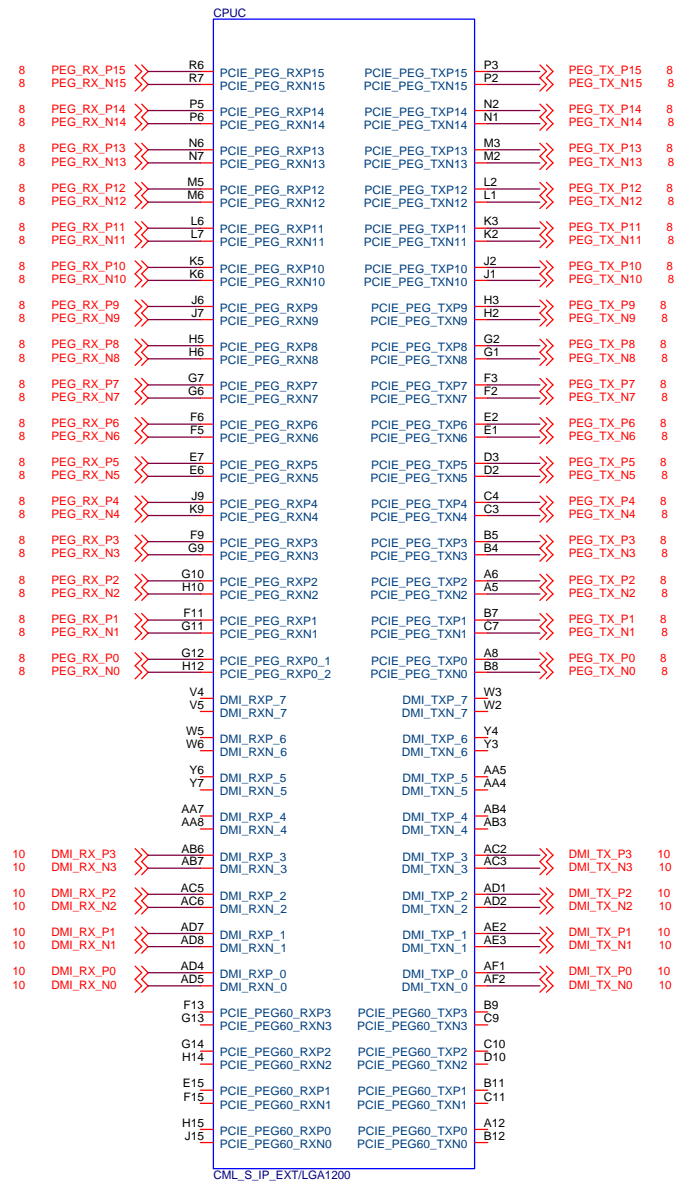
Intel® RST for PCIe Storage port configurable as x2/x4 M.2

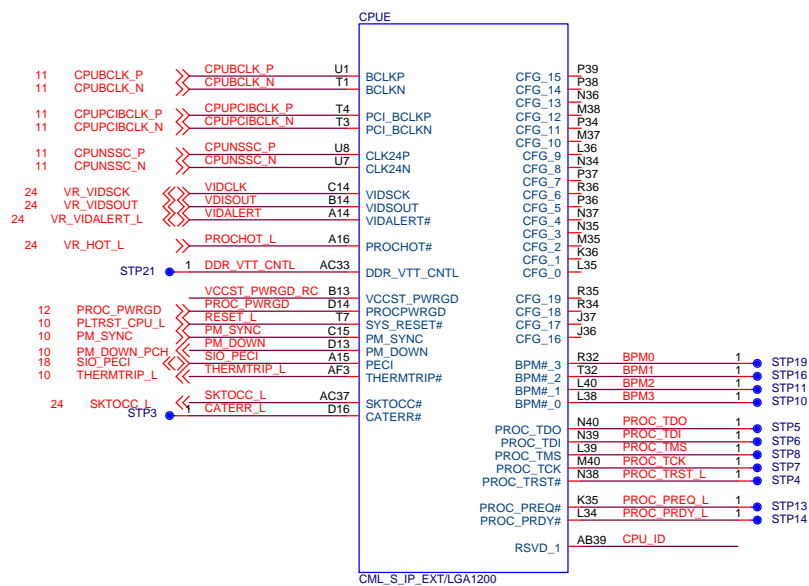
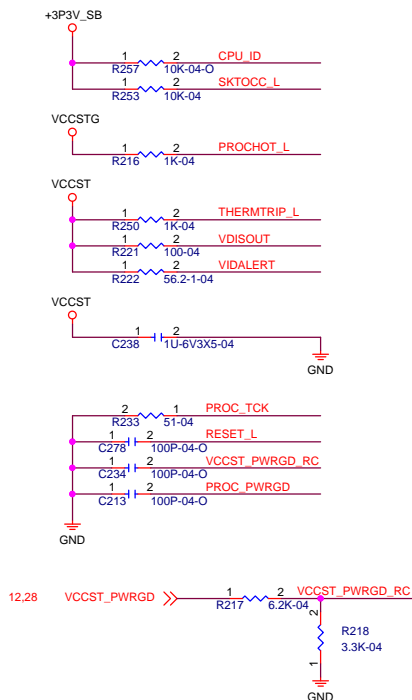
244mm

200mm



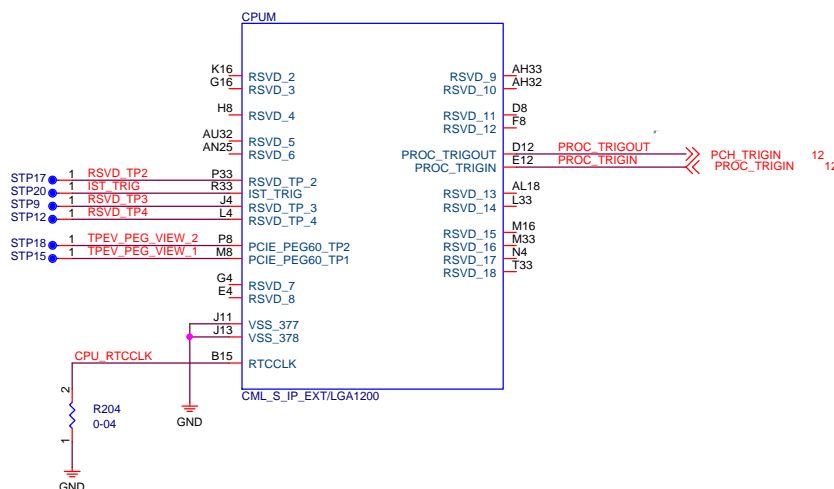






The CFG signals have a default value of '1' if not terminated on the board.

- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
 - 1 = (Default) Normal Operation; No stall.
 - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
 - 1 = Disabled.
 - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
 - 1 = (default) PEG Train immediately following RESET# de assertion.
 - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.



7 M.CLK_A.P[0..1] M.CLK_A.P[0..1]
7 M.CLK_A.N[0..1] M.CLK_A.N[0..1]
7 M.CS_A.L[0..1] M.CS_A.L[0..1]
7 M.CKE_A[0..1] M.CKE_A[0..1]
7 M.ODT_A[0..1] M.ODT_A[0..1]
7 M.MA_A[0..16] M.MA_A[0..16]
7 M.DATA_A[0..63] M.DATA_A[0..63]
7 M.DQS_A.P[0..7] M.DQS_A.P[0..7]
7 M.DQS_A.N[0..7] M.DQS_A.N[0..7]
7 M.BA_A0 M.BA_A0
7 M.BA_A1 M.BA_A1
7 M.BG_A0 M.BG_A0
7 M.BG_A1 M.BG_A1
7 M.PAR_A M.PAR_A
7 M.ACT_A.L M.ACT_A.L
7 M.ALT_A.L M.ALT_A.L
7 DDR_VREF_CA0 DDR_VREF_CA0

7 M.CLK_B.P[0..1] M.CLK_B.P[0..1]
7 M.CLK_B.N[0..1] M.CLK_B.N[0..1]
7 M.CS_B.L[0..1] M.CS_B.L[0..1]
7 M.CKE_B[0..1] M.CKE_B[0..1]
7 M.ODT_B[0..1] M.ODT_B[0..1]
7 M.MA_B[0..16] M.MA_B[0..16]
7 M.DATA_B[0..63] M.DATA_B[0..63]
7 M.DQS_B.P[0..7] M.DQS_B.P[0..7]
7 M.DQS_B.N[0..7] M.DQS_B.N[0..7]
7 M.BA_B0 M.BA_B0
7 M.BA_B1 M.BA_B1
7 M.BG_B0 M.BG_B0
7 M.BG_B1 M.BG_B1
7 M.PAR_B M.PAR_B
7 M.ACT_B.L M.ACT_B.L
7 M.ALT_B.L M.ALT_B.L
7 DDR_VREF_CA2 DDR_VREF_CA2

CPUA IL/NIL
DDR4 (IL)/DDR4 (NIL)
M.DATA_A57 AK1
M.DATA_A59 AH2
M.DATA_A61 AL1
M.DATA_A63 AH3
M.DATA_A62 AJ1
M.DATA_A60 AL3
M.DATA_A58 AH1
M.DATA_A56 AL2
M.DATA_A51 AN2
M.DATA_A49 AR1
M.DATA_A55 AN3
M.DATA_A53 AT2
M.DATA_A54 AP1
M.DATA_A52 AT3
M.DATA_A50 AN1
M.DATA_A48 AT1
M.DATA_A42 AV2
M.DATA_A43 AV1
M.DATA_A44 AV5
M.DATA_A41 AY4
M.DATA_A46 AW3
M.DATA_A47 AW2
M.DATA_A45 AY5
M.DATA_A40 AW5
M.DATA_A39 AW7
M.DATA_A35 AV7
M.DATA_A32 AW0
M.DATA_A33 AW9
M.DATA_A38 AY8
M.DATA_A34 AY7
M.DATA_A37 AV11
M.DATA_A36 AW11
M.DATA_A27 AW33
M.DATA_A26 AY33
M.DATA_A29 AW36
M.DATA_A25 AY35
M.DATA_A30 AY34
M.DATA_A31 AY33
M.DATA_A24 AY36
M.DATA_A28 AV36
M.DATA_A18 AV38
M.DATA_A19 AW38
M.DATA_A17 AT40
M.DATA_A16 AR38
M.DATA_A22 AU40
M.DATA_A23 AV39
M.DATA_A21 AR40
M.DATA_A10 AH40
M.DATA_A8 AK38
M.DATA_A9 AL40
M.DATA_A14 AM40
M.DATA_A15 AN39
M.DATA_A13 AK40
M.DATA_A12 AK39
M.DATA_A6 AG40
M.DATA_A2 AH40
M.DATA_A0 AE40
M.DATA_A1 AF40
M.DATA_A3 AH38
M.DATA_A7 AH39
M.DATA_A5 AE38
M.DATA_A4 AE39
DDR0_ECC_7
DDR0_ECC_6
DDR0_ECC_5
DDR0_ECC_4
DDR0_ECC_3
DDR0_ECC_2
DDR0_ECC_1
DDR0_ECC_0
ACB3
DDR_VREF_CA1
DDR_VREF_CA0
CML_S_IP_EXT/LGA1200

DDR4 (IL)/DDR4 (NIL)

DDR0_DQSP_7/DDR1_DQSP_7

DDR0_DQSN_7/DDR1_DQSN_7

DDR0_DQSP_6/DDR1_DQSP_6

DDR0_DQSN_6/DDR1_DQSN_6

DDR0_DQSP_5/DDR1_DQSP_5

DDR0_DQSN_5/DDR1_DQSN_5

DDR0_DQSP_4/DDR1_DQSP_4

DDR0_DQSN_4/DDR1_DQSN_4

DDR0_DQSP_3/DDR1_DQSP_3

DDR0_DQSN_3/DDR1_DQSN_3

DDR0_DQSP_2/DDR1_DQSP_2

DDR0_DQSN_2/DDR1_DQSN_2

DDR0_DQSP_1/DDR1_DQSP_1

DDR0_DQSN_1/DDR1_DQSN_1

DDR0_DQSP_0/DDR1_DQSP_0

DDR0_DQSN_0/DDR1_DQSN_0

DDR0_ACT#_2

DDR0_PAR

DDR0_ALERT#

DDR0_DQSP_7/DDR1_DQSP_7

DDR0_DQSN_7/DDR1_DQSN_7

DDR0_DQSP_6/DDR1_DQSP_6

DDR0_DQSN_6/DDR1_DQSN_6

DDR0_DQSP_5/DDR1_DQSP_5

DDR0_DQSN_5/DDR1_DQSN_5

DDR0_DQSP_4/DDR1_DQSP_4

DDR0_DQSN_4/DDR1_DQSN_4

DDR0_DQSP_3/DDR1_DQSP_3

DDR0_DQSN_3/DDR1_DQSN_3

DDR0_DQSP_2/DDR1_DQSP_2

DDR0_DQSN_2/DDR1_DQSN_2

DDR0_DQSP_1/DDR1_DQSP_1

DDR0_DQSN_1/DDR1_DQSN_1

DDR0_DQSP_0/DDR1_DQSP_0

DDR0_DQSN_0/DDR1_DQSN_0

DDR0_DQSP_8

DDR0_DQSN_8

DDR0_DQSP_9

DDR0_DQSN_9

DDR0_DQSP_10

DDR0_DQSN_10

DDR0_DQSP_11

DDR0_DQSN_11

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DDR0_DQSP_112

DDR0_DQSN_112

DDR0_DQSP_113

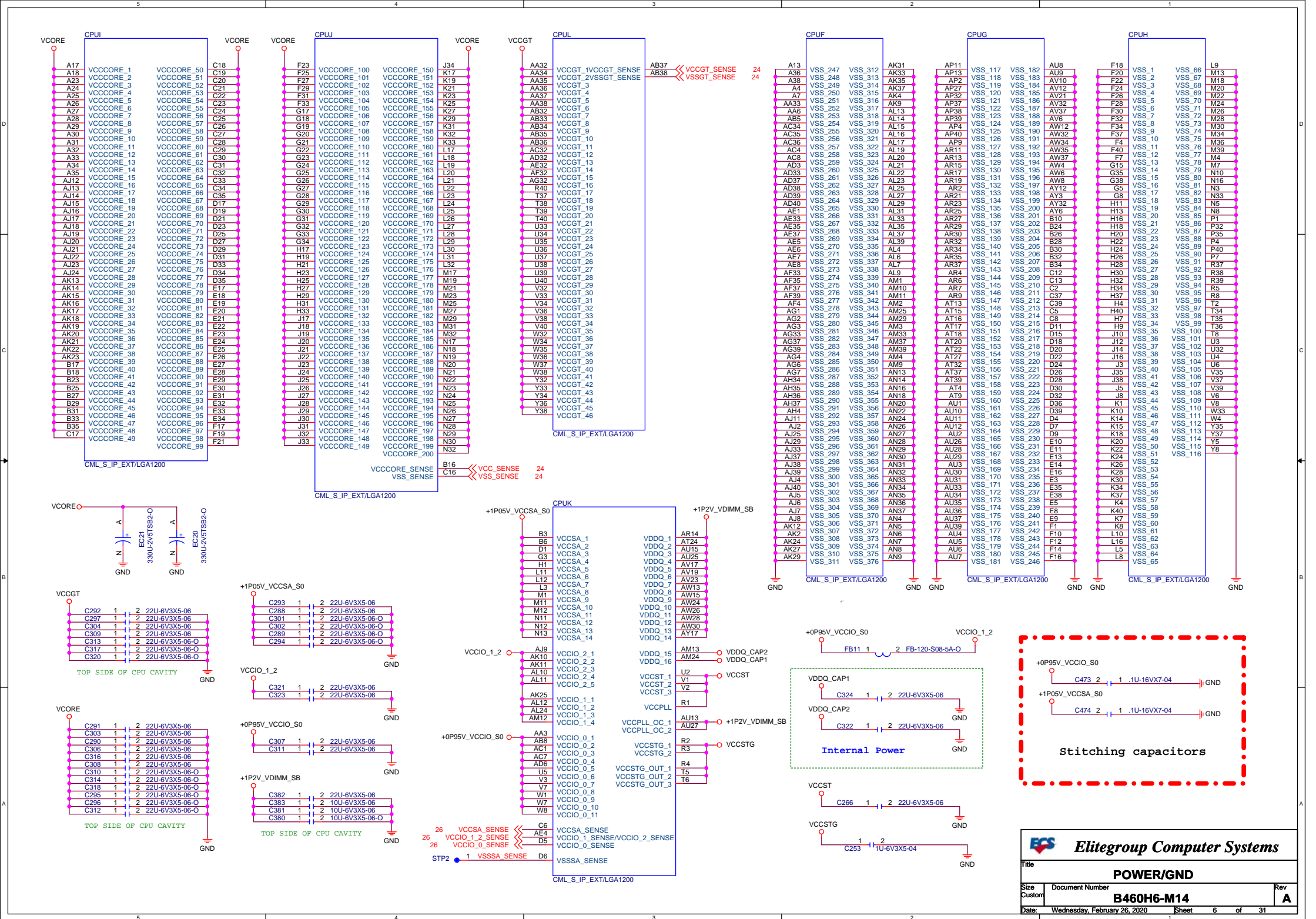
DDR0_DQSN_113

DDR0_DQSP_114

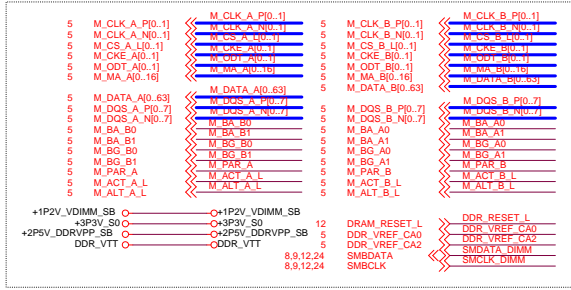
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DDR0_DQSP_115

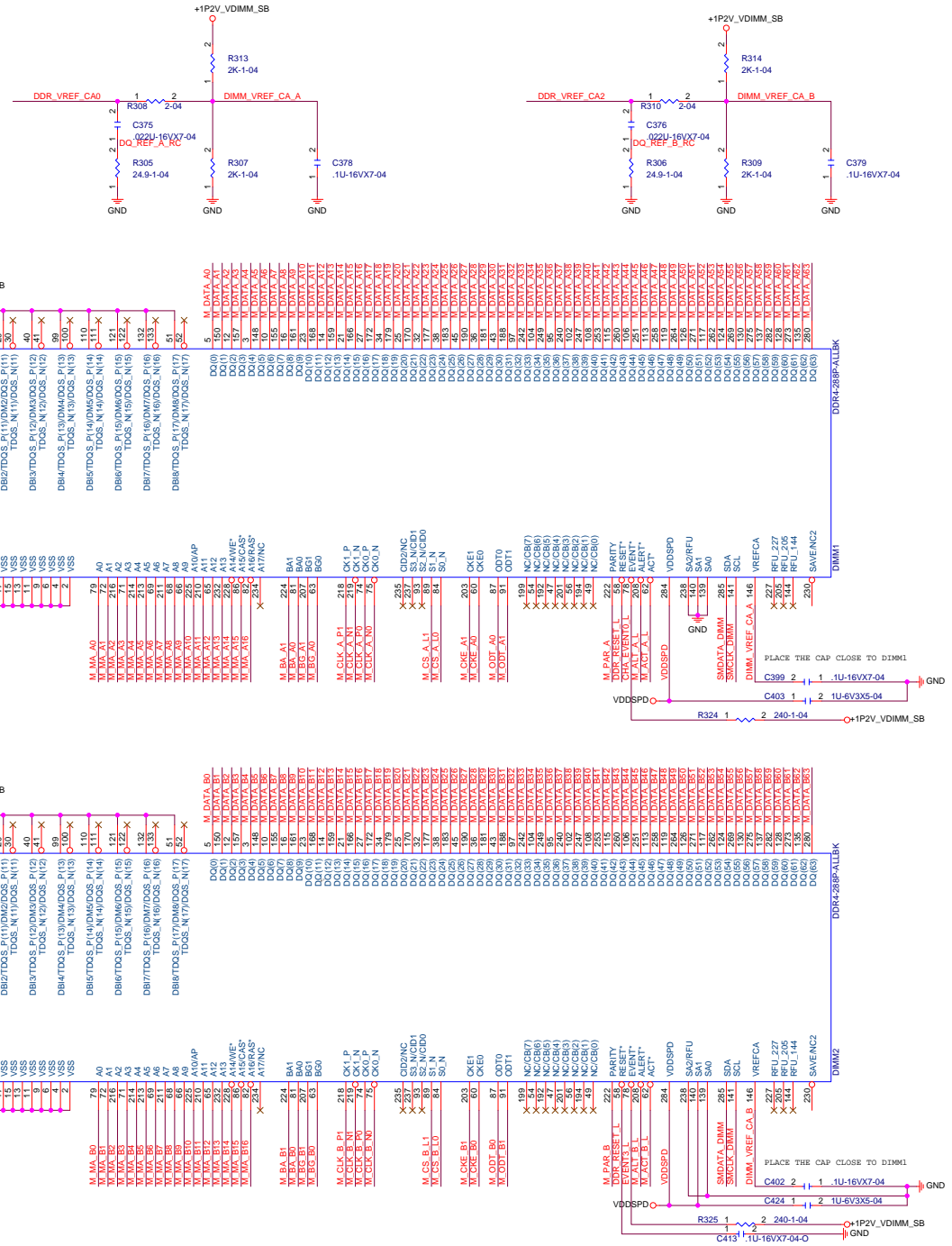
DDR0_DQSN_115



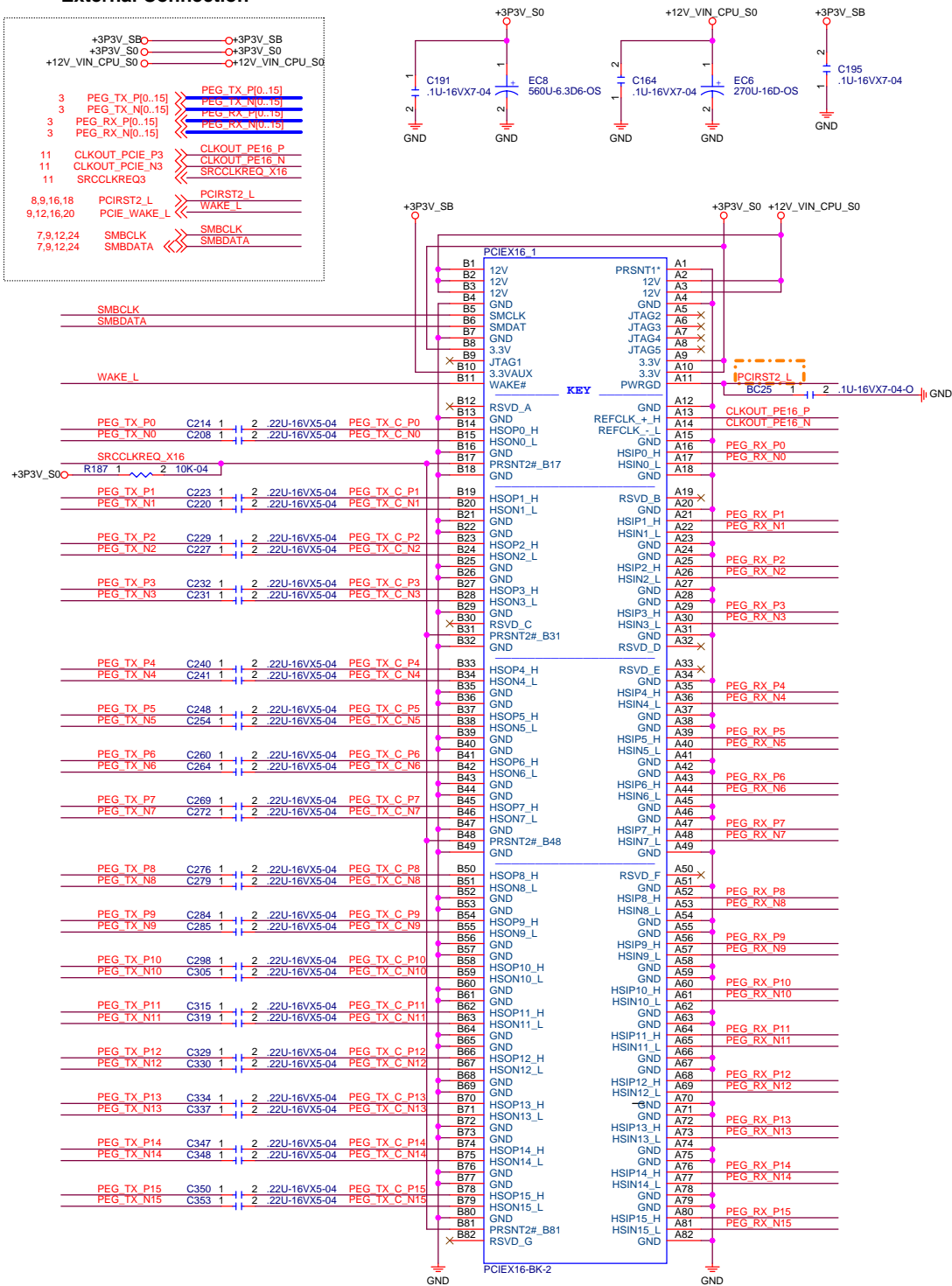
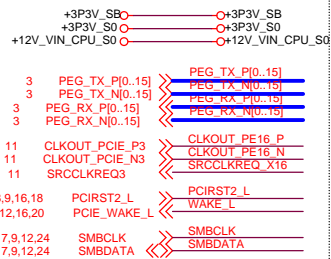
External Connection



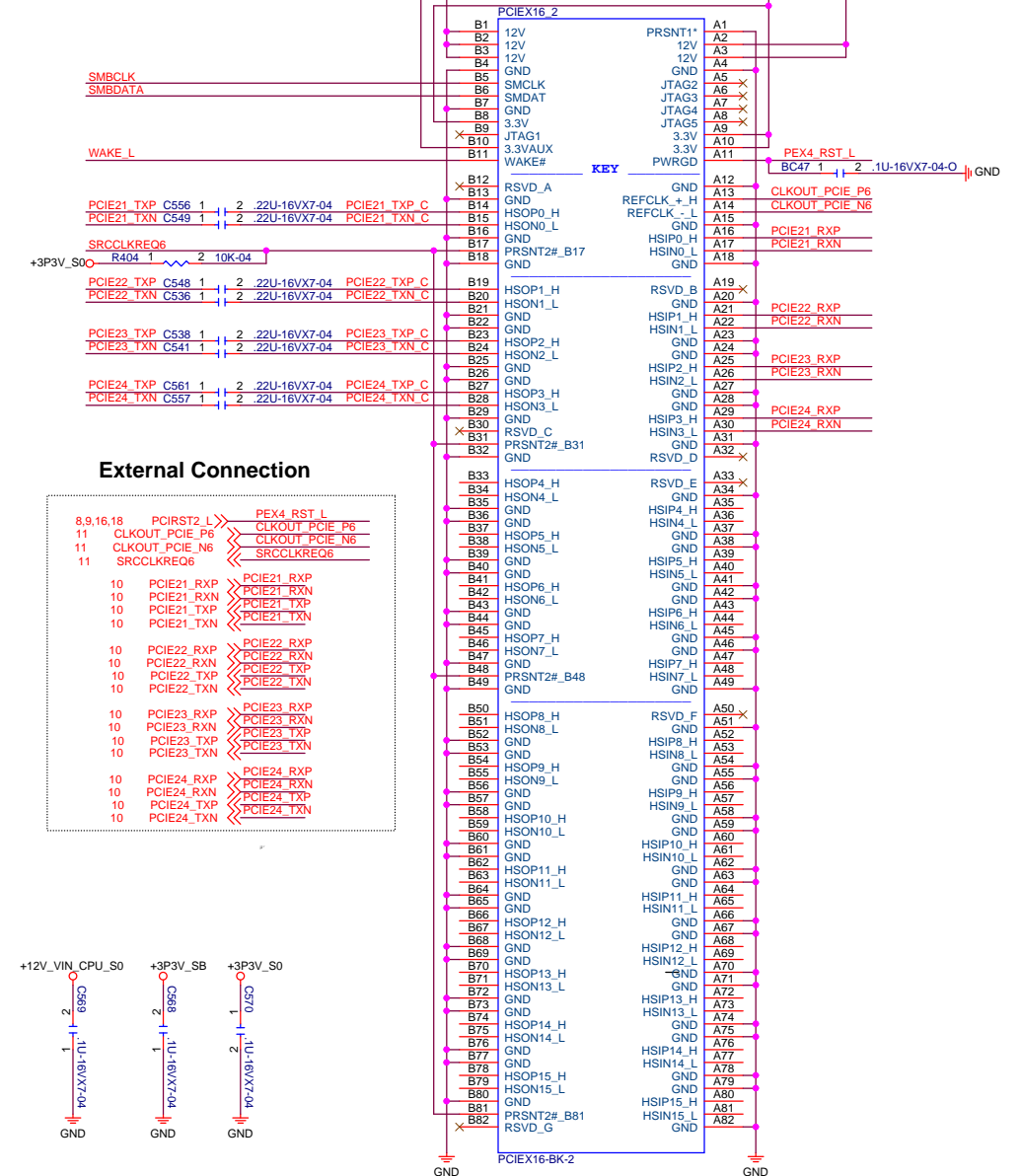
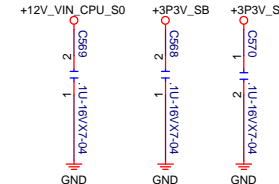
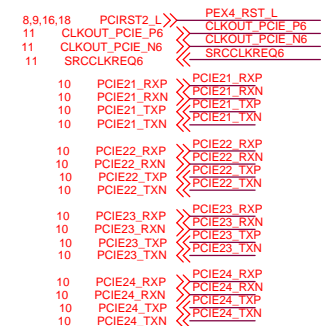
SPD address
DIMM1 A0
DIMM2 A4



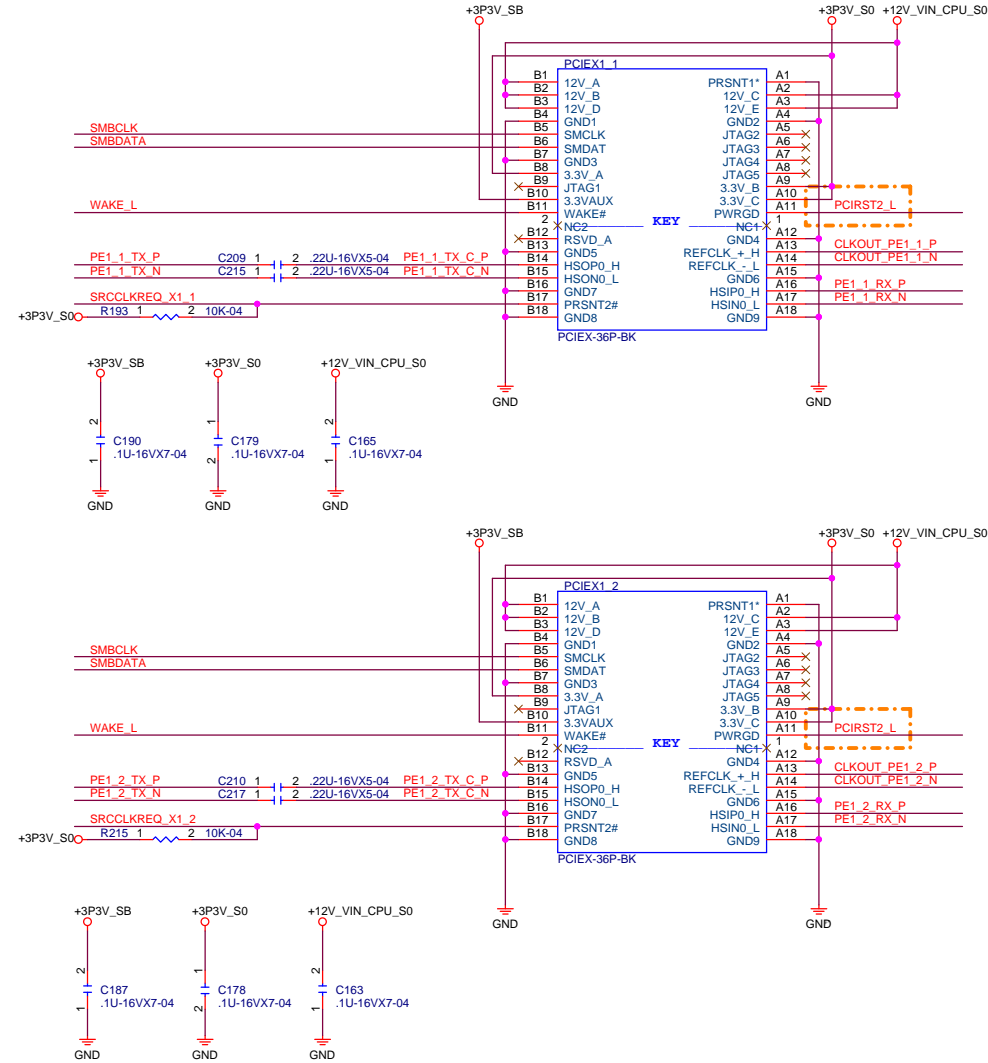
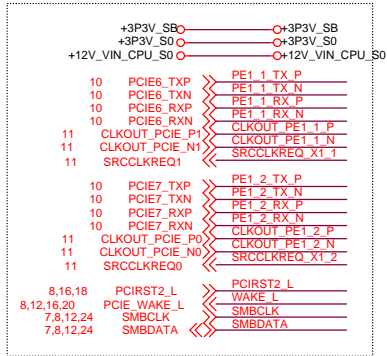
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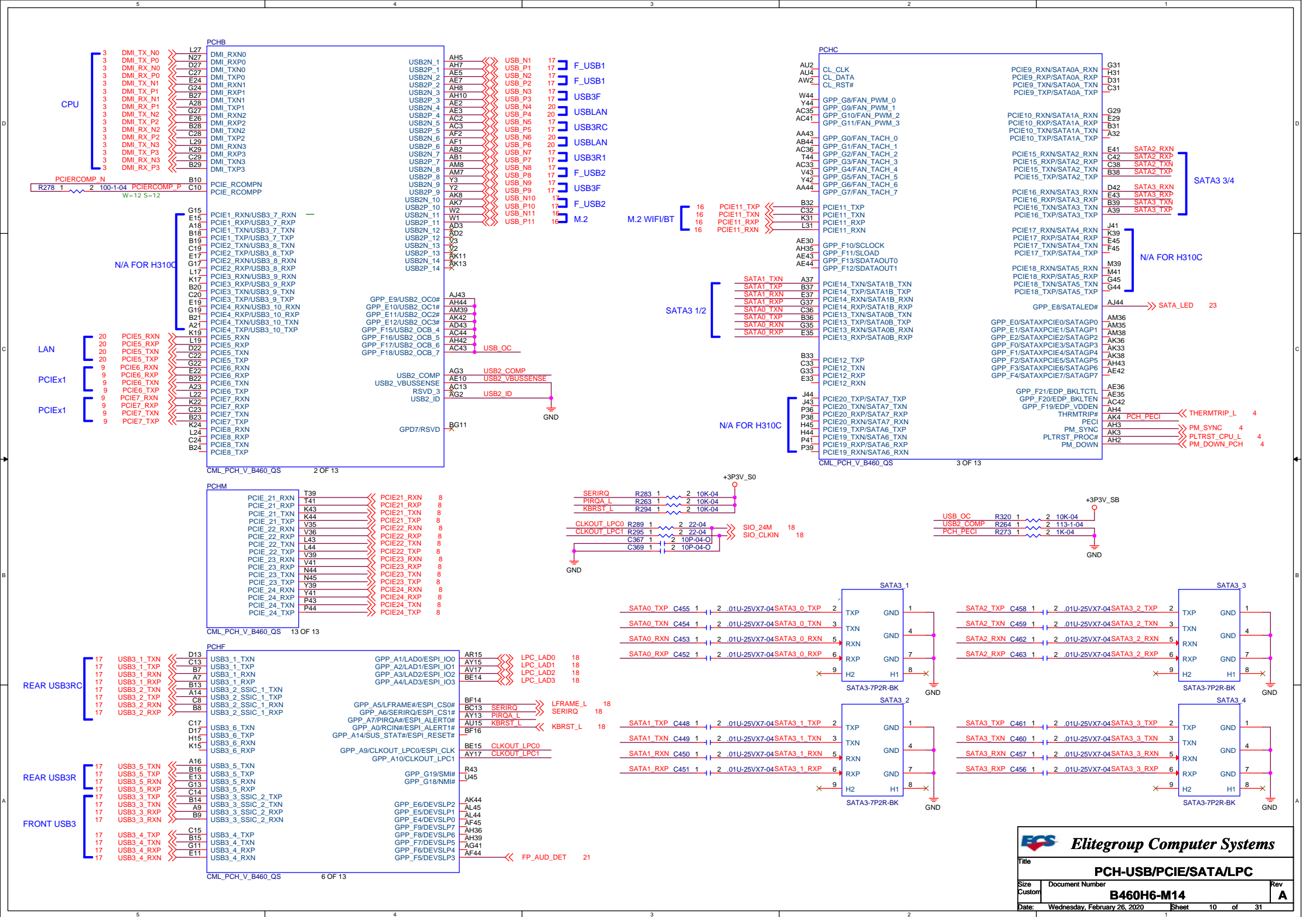


External Connection



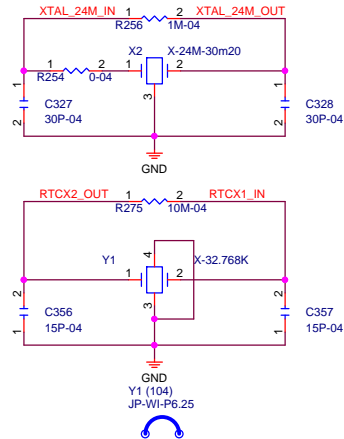
External Connection



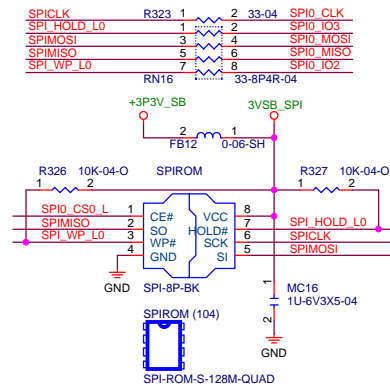


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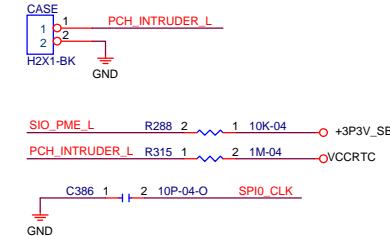
XTAL



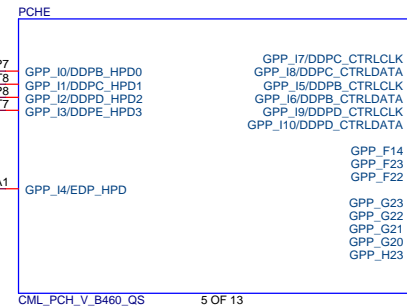
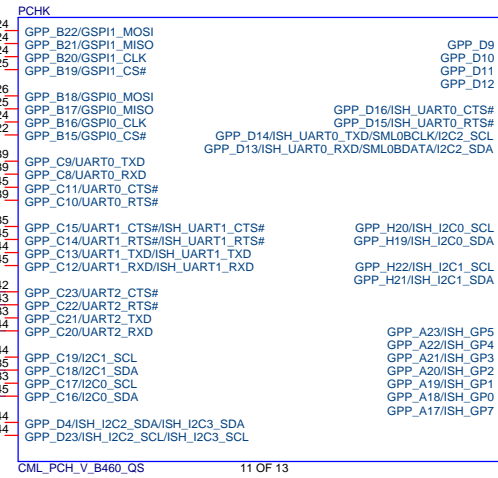
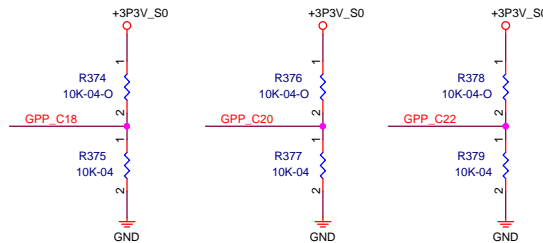
BIOS ROM

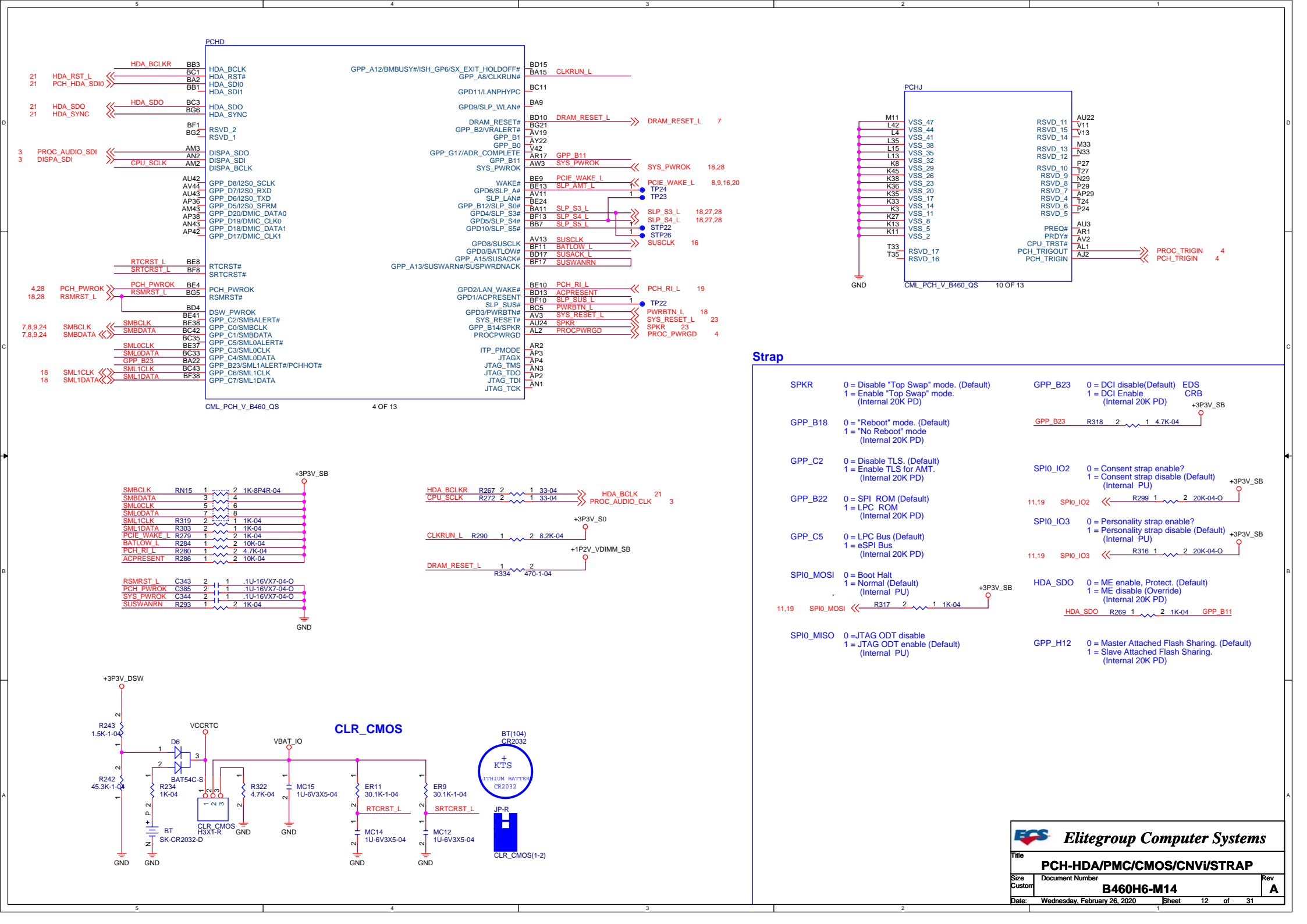


CASE OPEN



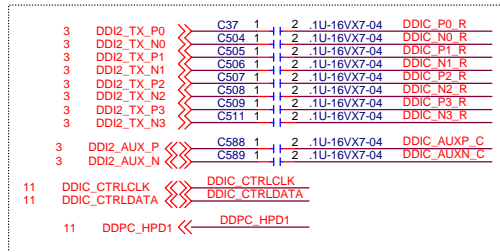
BOM SELECTION





Pin 11 connection diagram for the DDI01 module. The diagram shows the following connections:

- VCC (+12V_VIN_CPU_S0, +3P3V_S0, +VCC_HDMI) connected to +5V_S0, +12V_VIN_CPU_S0, +3P3V_S0, and +VCC_HDMI.
- DDI01_TX_P0 through DDI01_TX_P3 connected to DDI HDMI P0 through P3.
- DDI01_TX_N0 through DDI01_TX_N3 connected to DDI HDMI N0 through N3.
- DDI01_CTRLCLK connected to DDI01_CTRLCLK.
- DDI01_CTRLDATA connected to DDI01_CTRLDATA.
- DDI01_HPD connected to DDI01_HPD.



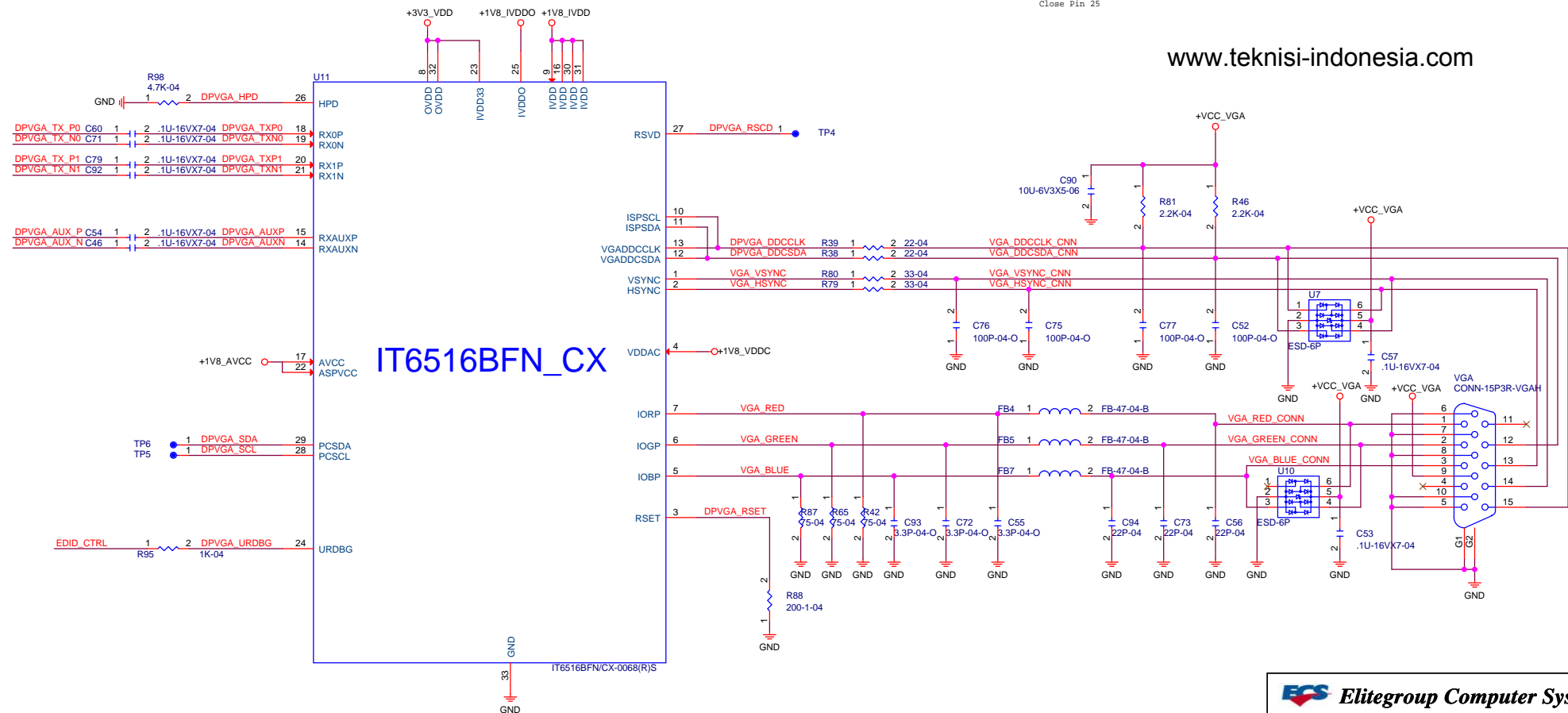
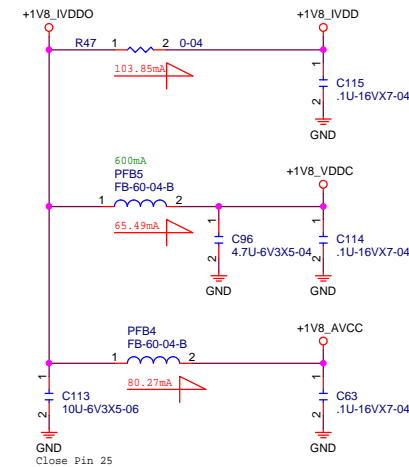
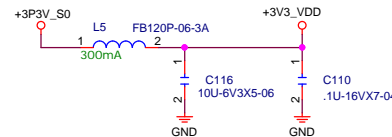
The schematic diagram illustrates the internal circuitry of the DP connector for the ESD-10P-USB30-0 module. It shows the connection between the module's pins and the external DP connector pins. Key components include MOSFETs QN26 and QN27, resistors R389 and R390, and various capacitors. The circuit is powered by +3P3V_S0, +12V_VIN_CPU_S0, and +DP_VCC3. It includes connections for DDIC (Data Dwell Interconnect) signals, DDPC (Data Dwell Protection Control) signals, and auxiliary signals like AUX_P and AUX_N. The DP connector is a 20-pin connector with pins 1 through 20 labeled. The module pins are labeled with their respective functions, such as I/O1, I/O2, I/O3, and I/O4. The diagram also shows the connection to the ESD-10P-USB30-0 module pins.

External Connection

+VCC_HDMI ○ +VCC_VGA
+3P3V_S0 ○ +3P3V_S0

3 DDI3_TX_P0 >> DPVGA_TX_P0
3 DDI3_TX_N0 >> DPVGA_TX_N0
3 DDI3_TX_P1 >> DPVGA_TX_P1
3 DDI3_TX_N1 >> DPVGA_TX_N1
3 DDI3_AUXP >> DPVGA_AUX_P
3 DDI3_AUXN >> DPVGA_AUX_N
11 DDPD_HPDI >> DPVGA_HPDI
11 EDID_CTRL >> EDID_CTRL

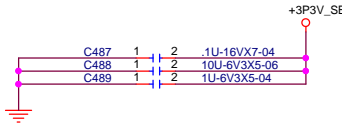
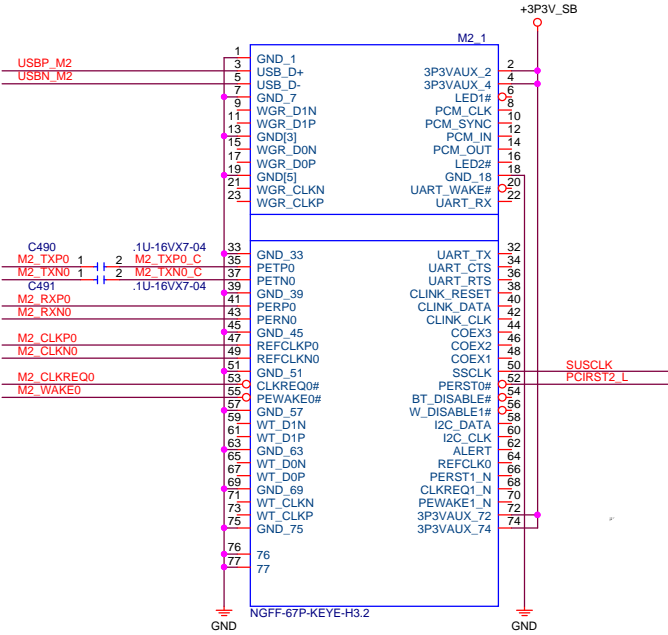
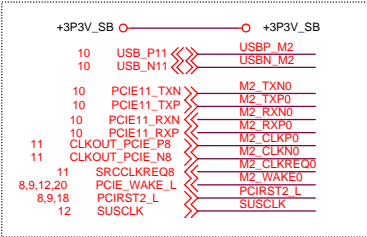
GPO control EDID behavior for KVM issue
DOS mode: High, report default EDID
Win mode: Low, report real monitor EDID



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M.2 2230 WiFi / BT

External Connection



2230BS
M2_BOSS_H1.45
GND

M2_BOSS WITH STUB
22-232-203300
23-745-201155



2230BS(104)
M2_SCREW_D4.8

M2_SCREW:
22-232-203300
22-232-200327

COM1

COM2

FAN

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-45		0	DSW
JP2	WDT_EN	1	Disable WDT to reset FWOK
Pin-46		0	Enable WDT to reset FWOK
JP3	Vih/Vil_SEL	1	3.3V Level (Default)
Pin-121		0	1.8V Level
JP4	KSPWR_EN	1	Disable K3 Power Sequence
Pin-123		0	Enable K3 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6		1	Enable LPC Interface
Pin-119	LPC/eSPI	0	Enable eSPI Interface
JP7		1	Disable DDR4
Pin-55	DDR4_EN	0	Enable DDR4

PWRC

RESET

LPC

SMBUSPS2

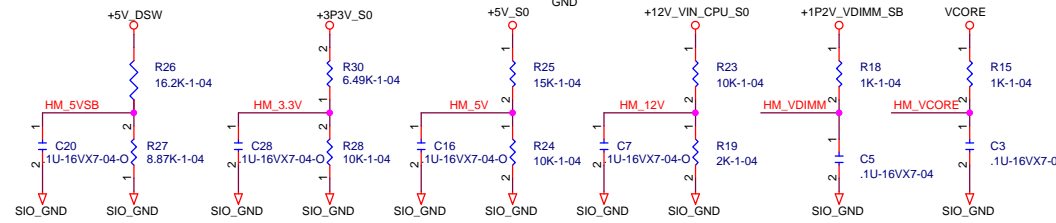
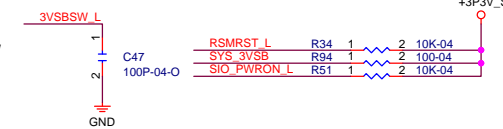
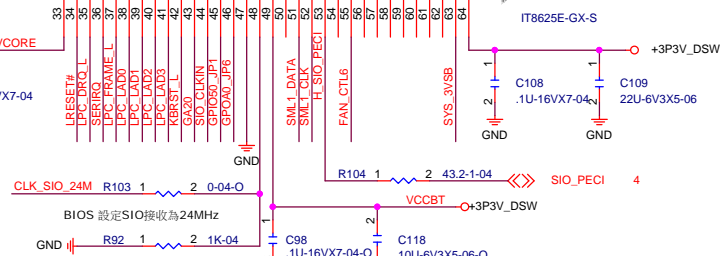
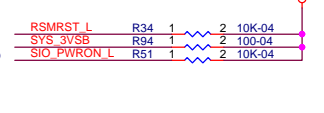
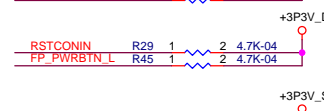
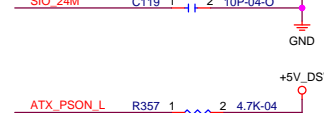
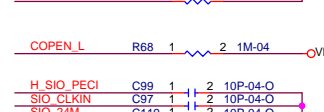
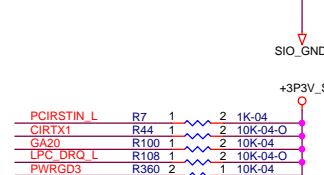
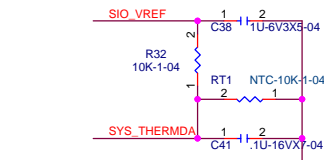
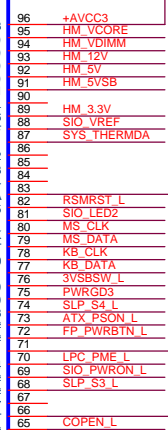
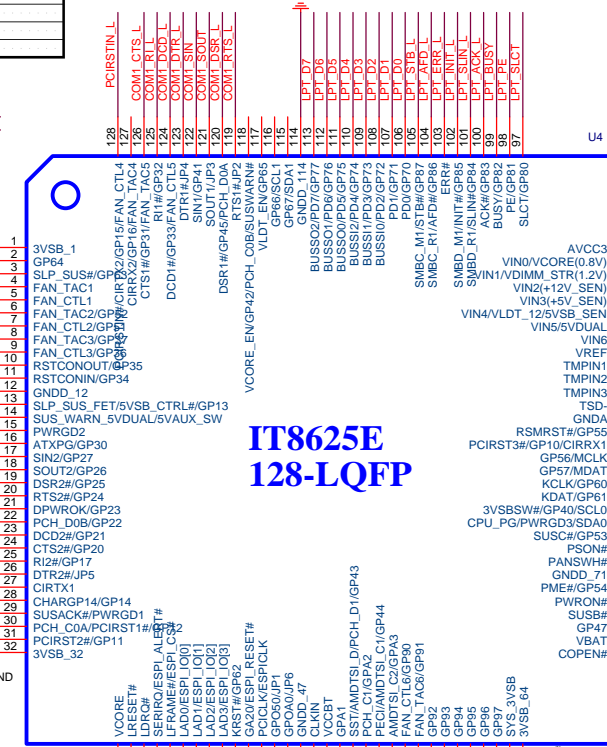
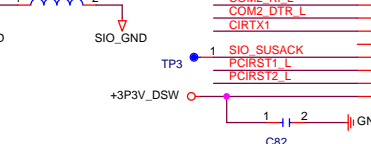
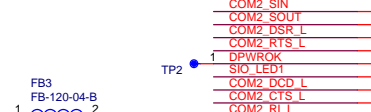
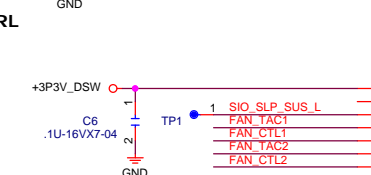
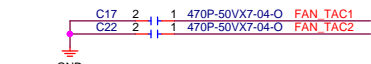
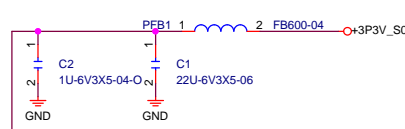
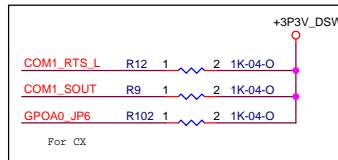
LPT

GPI O

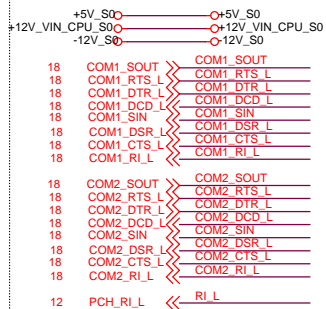
JP3 COM1 SOL R10 1 2 1K-04
JP4 COM1 DTR L R91 1 2 1K-04
JP6 COM1 RTS L R11 1 2 1K-04
JP7 FAN CTL6 R93 1 2 1K-04

JP2 GP0A0 JP6 R91 1 2 1K-04
JP5 COM2 DTR L R36 1 2 1K-04

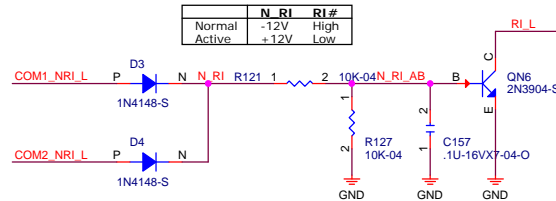
JP1 GPIO0_JP1 R101 1 2 1K-04
R107 1 2 8.2K-04-0
GND



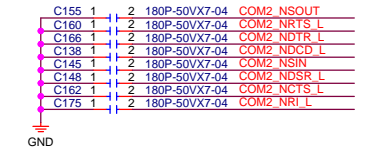
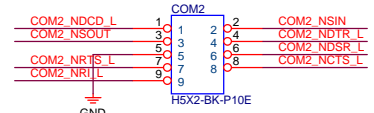
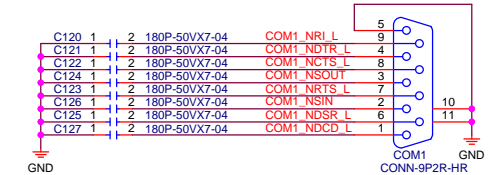
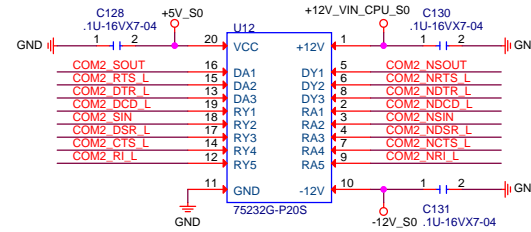
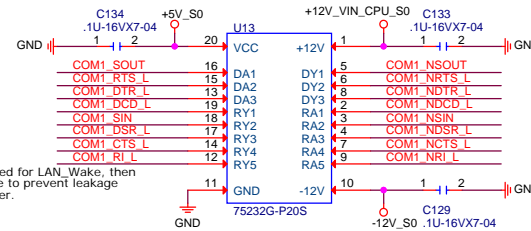
External Connection



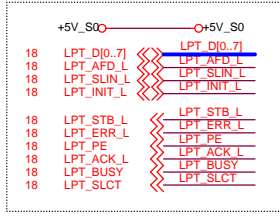
COM Header+Connector



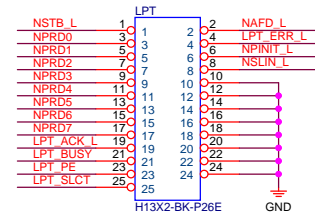
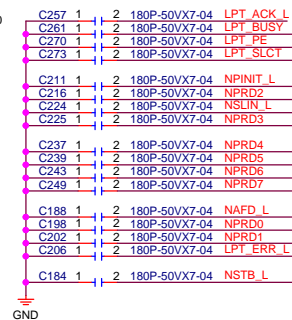
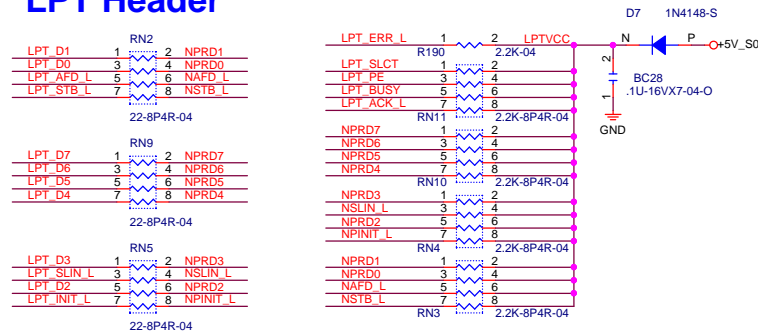
If COM1_RI used for LAN_Wake, then need add diode to prevent leakage current to buffer.



External Connection



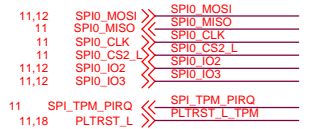
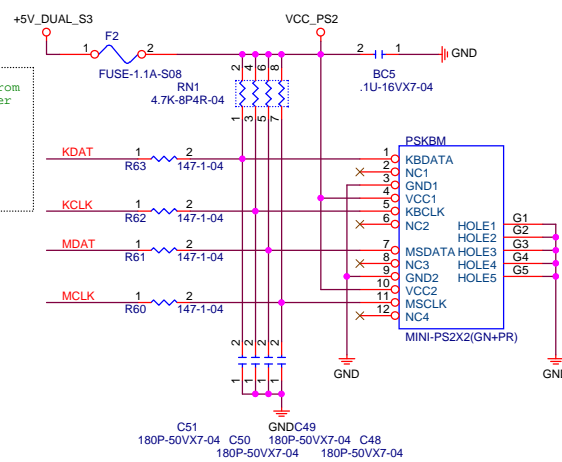
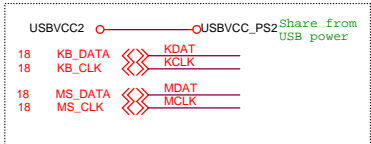
LPT Header



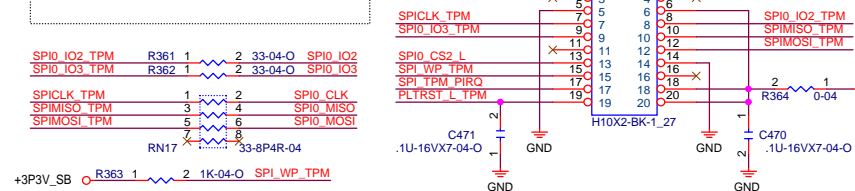
PS2

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External Connection



SPI TPM header

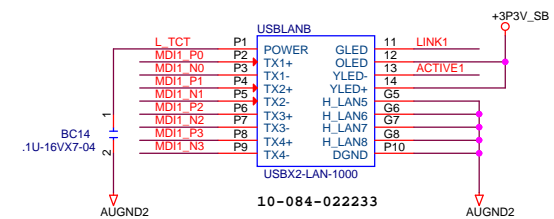
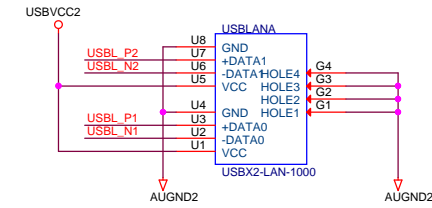
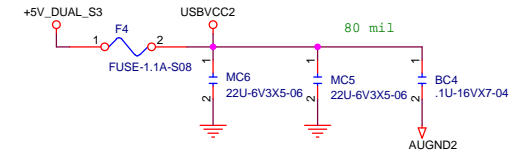
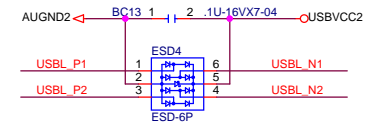
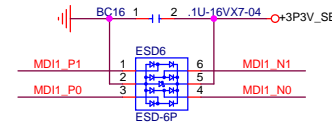
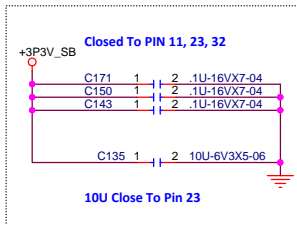
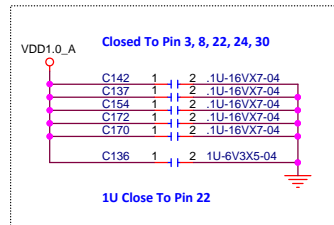
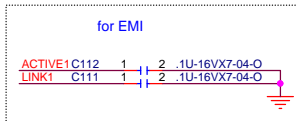
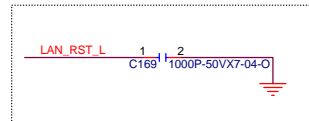
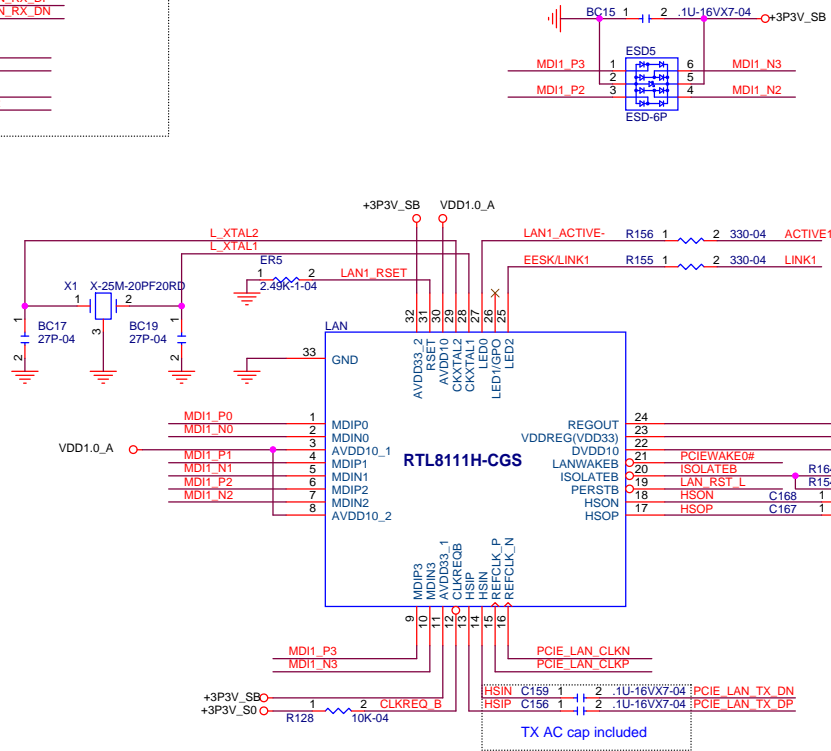
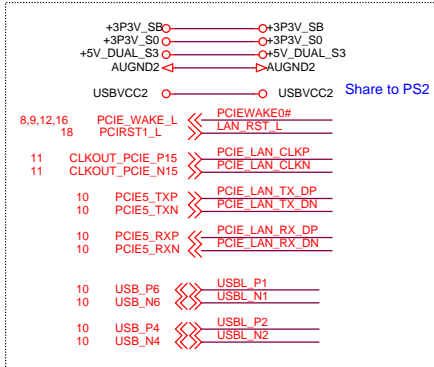


A dual-row, 20-pin R.A. female connector:

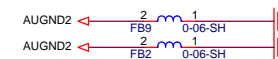
Pin	Name	Pin	Name
1	KEYWAY	2	N.C.
3	N.C. ¹	4	N.C.
5	GND	6	VDD3V3
7	SCLK ²	8	N.C.
9	N.C.	10	MISO
11	N.C.	12	MOSI
13	SCS ³	14	GND
15	N.C.	16	N.C.
17	SPI_I/O ⁴	18	VSB3V3
19	SPI_RST ⁴	20	N.C.

NUVOTON

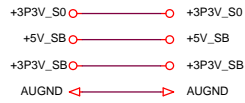
External Connection



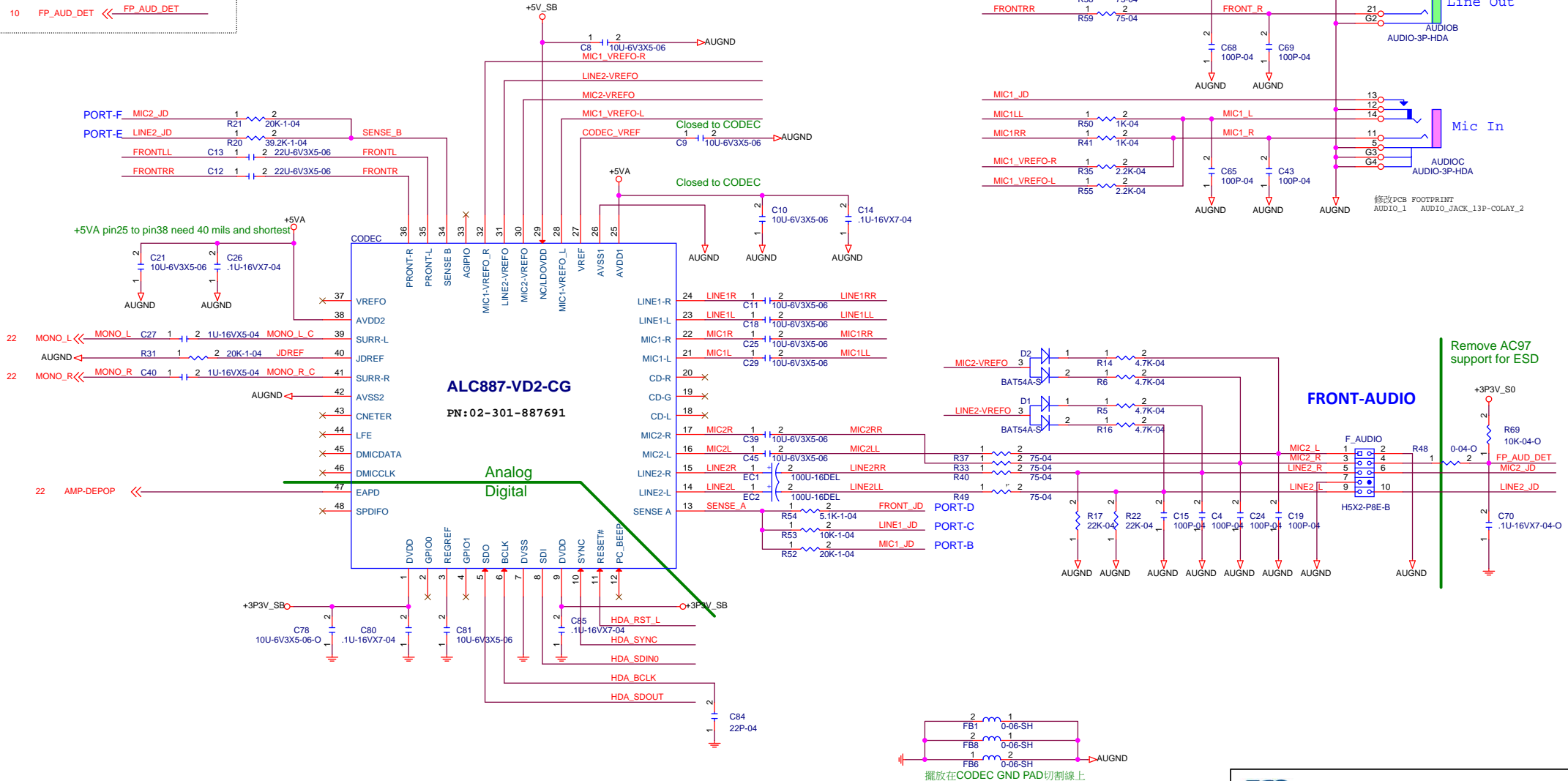
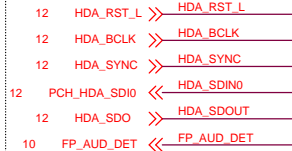
Link: Green on
Active: Yellow blinking



External Connection

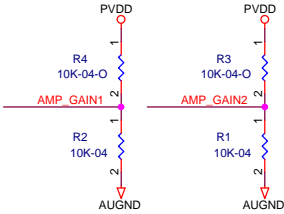
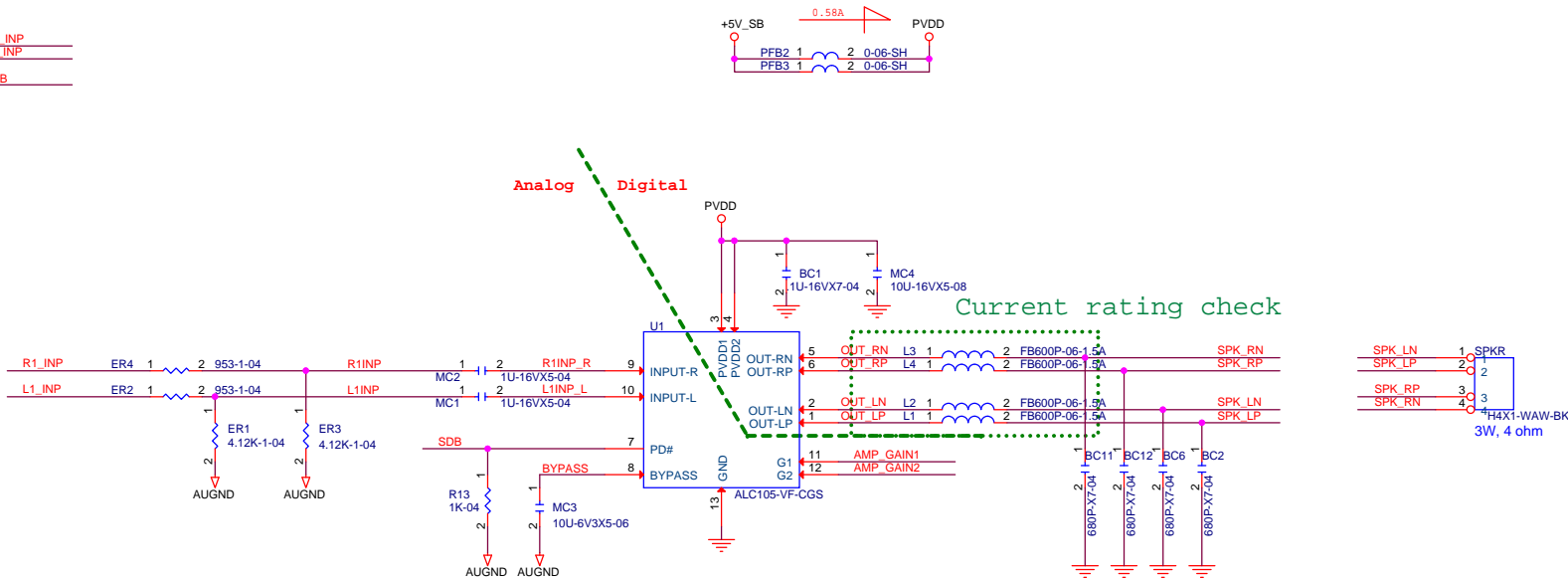


螺絲孔



Amplifier ALC105

- 21 MONO_R >> R1_INP
- 21 MONO_L >> L1_INP
- 21 AMP-DEPOP >> SDB

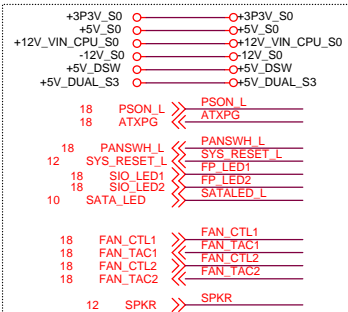


*

Output Gain Table

G2	G1	SE-input Stereo-output Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

External Connection



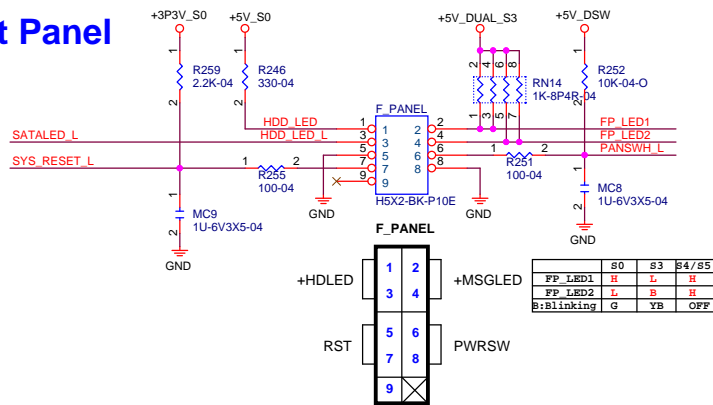
Front Panel

ATX_PWR

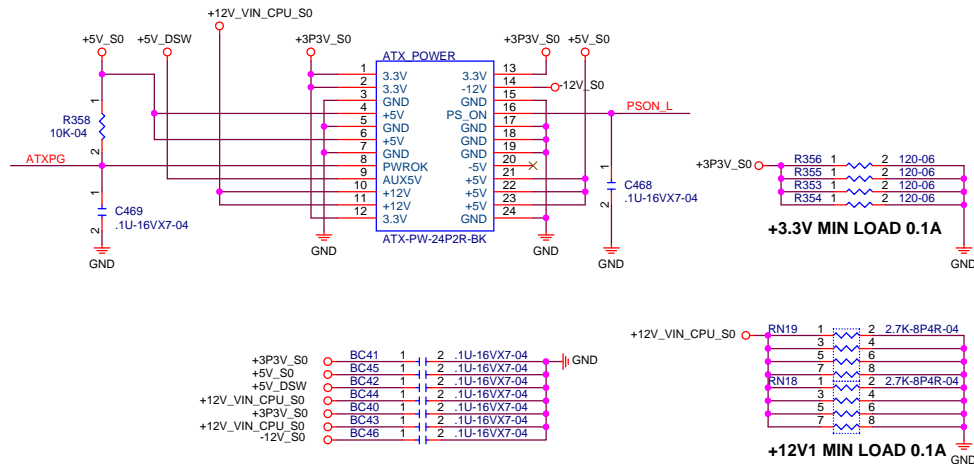
Front Panel

FAN

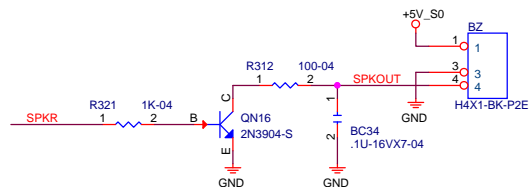
Buzzer



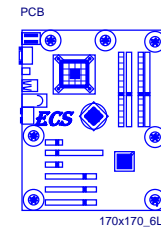
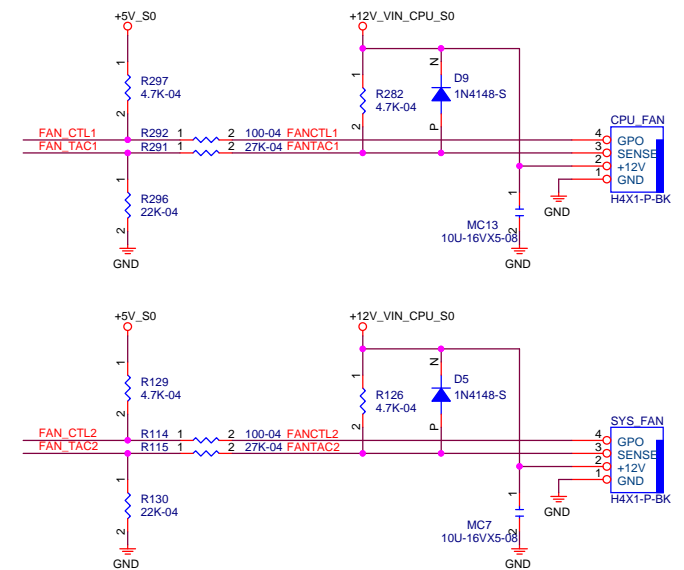
ATX CONNECTOR



BUZZER HEADER



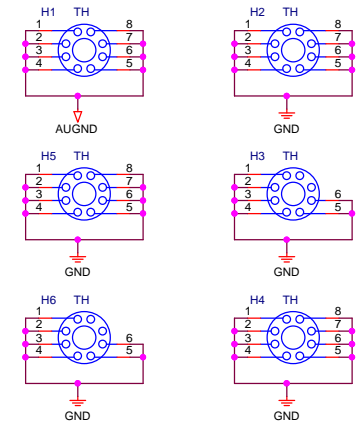
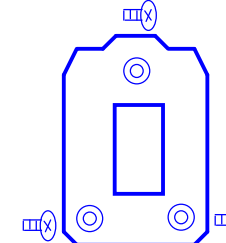
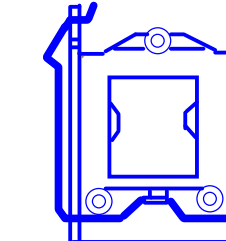
FANS

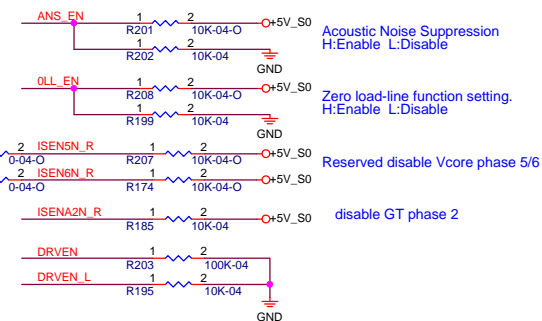


Hole/ PCB/104

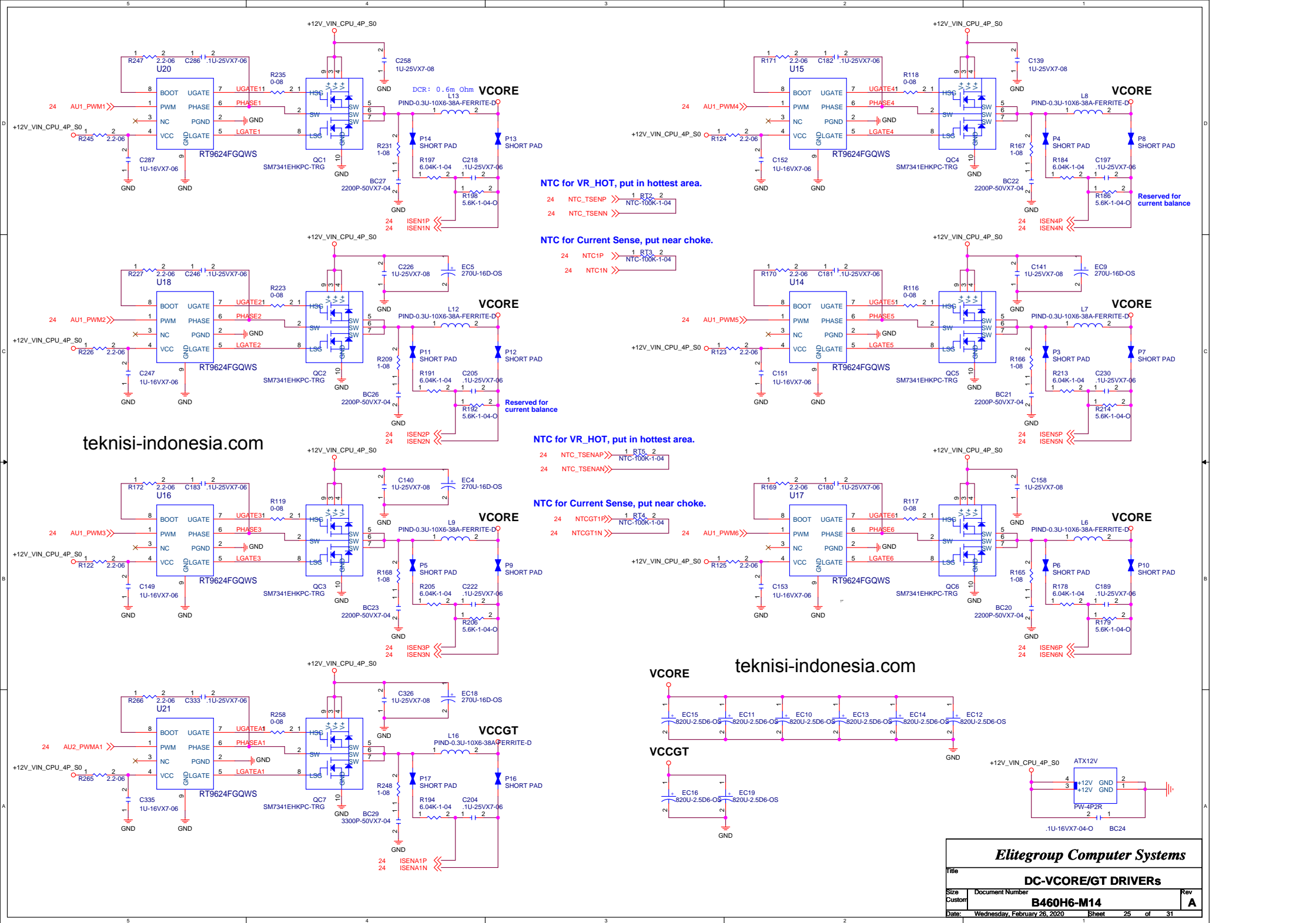
305 * 244 = 9 Hole (1+8)
 244 * 244 = 8 Hole (1+7)
 305 * 220-170 = 6 Hole (1+5)
 244-220 * 220-170 = 6 Hole (1+5)
 210-170 * 220-170 = 4 Hole (1+3)

CPU 115X-RM





Loadline: $LL = DCR \cdot R_{\text{mon-eq}} \cdot R_{1fb}/3/R_{\text{sen}}/R_{2fb}$, R_{2fb} = which connect COMP



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	OUTPUT	OUTPUT	OUTPUT
S3	L	H	OUTPUT	OUTPUT	HIGH-Z
S4/ S5	L	L	DISCHARGE	DISCHARGE	DISCHARGE

OCP 太高

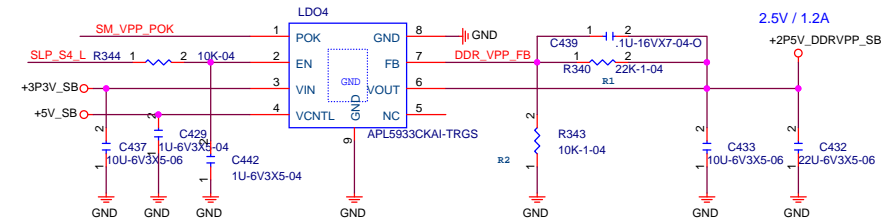
DDR_VPP

5VDUAL

TOTAL: 16.5A/1A

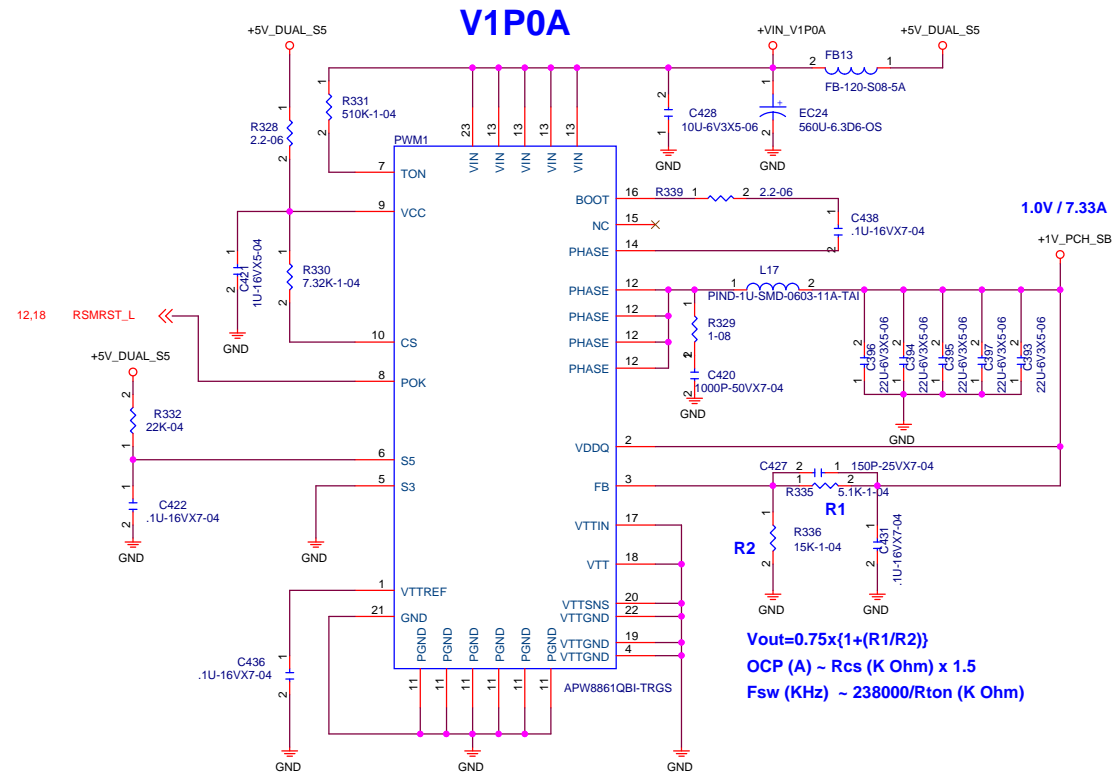
	S0	S3	S4/S5
3VBSBW_L	H	L	H
5VDUAL	VCC	5VSB	0V

	S0	S3	S4/S5
3VBSW_L	H	L	H
5VDUAL	VCC	5VSB	0V



[illegible]

	S0	S3/S4/S5
SYS_PWROK	H	L
5VDUALS5	VCC	5VSB



$V_{out} = 0.75 \times \{1 + (R_1/R_2)\}$
 $OCP (A) \sim R_{cs} (K \Omega) \times 1.5$
 $F_{sw} (KHz) \sim 238000/R_{ton} (K \Omega)$

12,18,27

SLP_S4_L

R232

10K-04

QN9
SM2300NSAC-TRG-S
4.5V $R_{ds(on)}=30m$

+1V_PCH_SB

R229
0-04-O

1 2

G

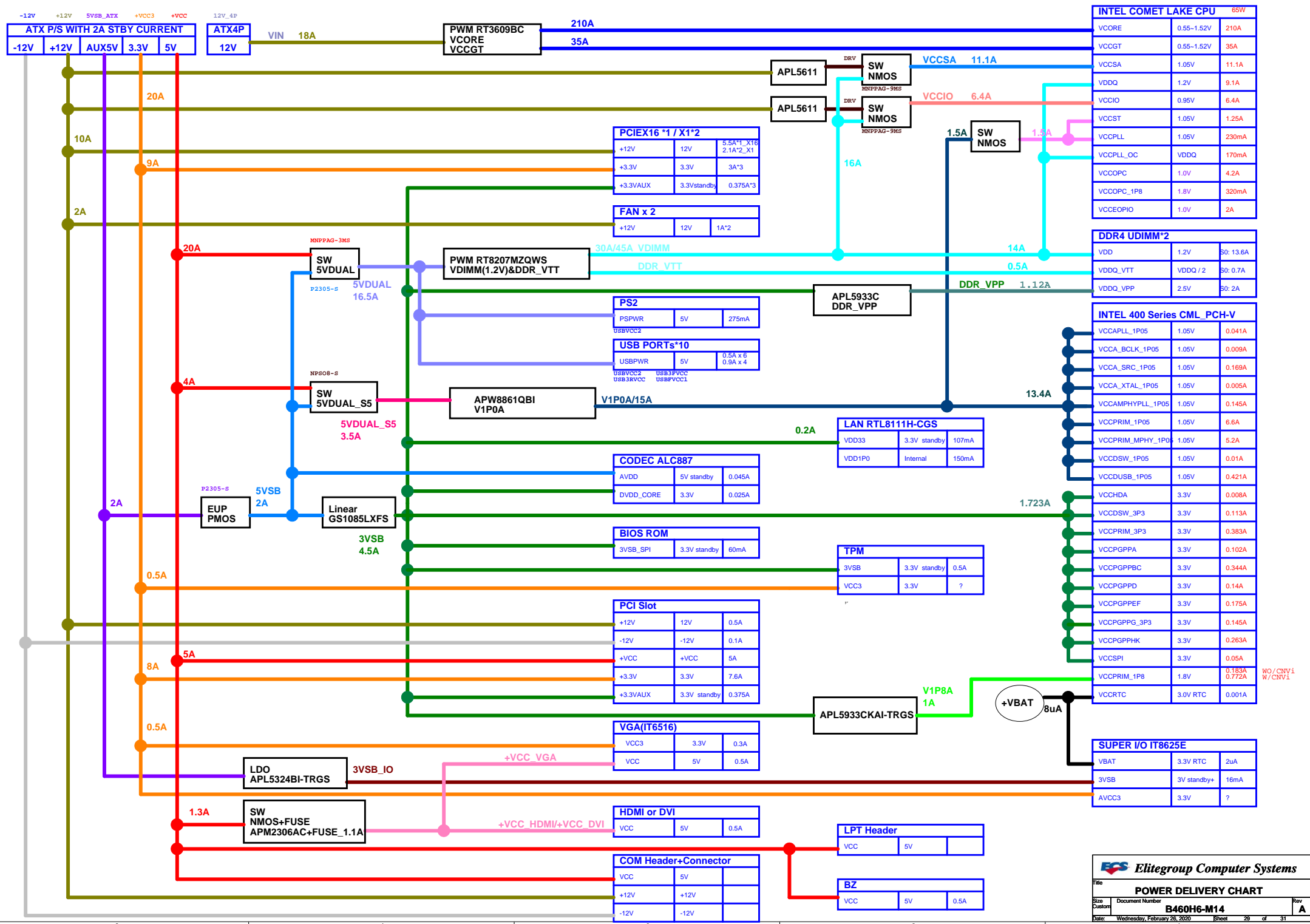
C267
1U-16VX7-0

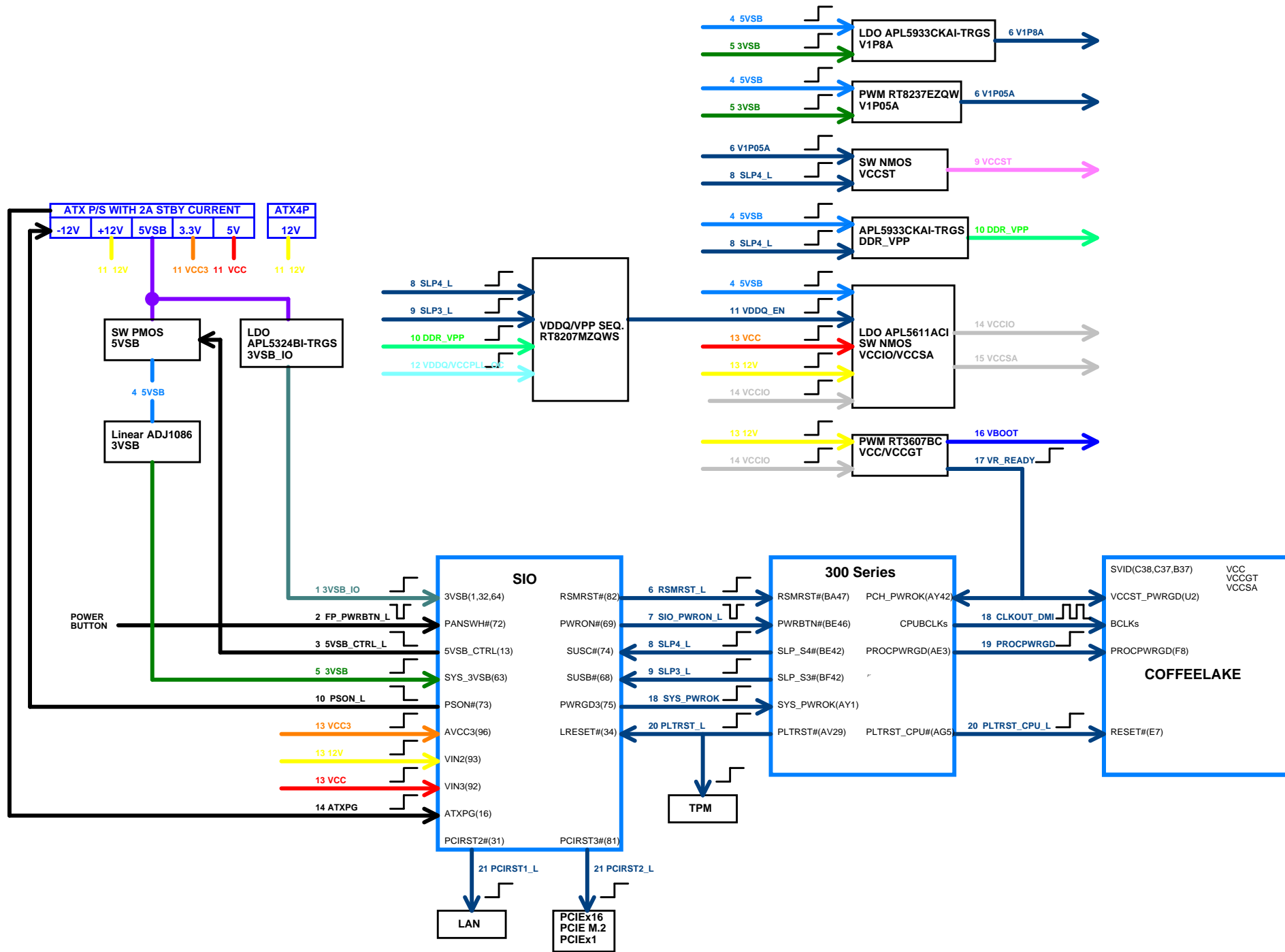
C265
22U-6V3X5-06

VCCST

1.05V / 0.265A

GND





DIMM

Name	CH	SPD address
DIMM1	Channel A	0xA0
DIMM2	Channel B	0xA4

DDI

Name	Type	Port	DDC	AUX
DDI1	HDMI	PortB	PortB	N/A
DDI2	DVI	PortC	PortC	N/A
DDI3(VGA)	DP	PortD	N/A	PortD

Clock	Function	Mapping	CLKREQ
CLOCKOUT_ITPXD	Disable	N/A	N/A
CLOCKOUT_PCIE_0	PCIEX1	CLKREQ0	Enable
CLOCKOUT_PCIE_1	PCIEX1	CLKREQ1	Enable
CLOCKOUT_PCIE_2	Disable	CLKREQ2	Disable
CLOCKOUT_PCIE_3	PCIEX16	CLKREQ3	Enable
CLOCKOUT_PCIE_4	Disable	CLKREQ4	Disable
CLOCKOUT_PCIE_5	Disable	CLKREQ5	Disable
CLOCKOUT_PCIE_6	PCI BREDGE	CLKREQ6	Disable
CLOCKOUT_PCIE_7	Disable	CLKREQ7	Disable
CLOCKOUT_PCIE_8	M.2 SSD	CLKREQ8	Disable
CLOCKOUT_PCIE_9	Disable	CLKREQ9	Disable
CLOCKOUT_PCIE_10	Disable	CLKREQ10	Disable
CLOCKOUT_PCIE_11	Disable	CLKREQ11	Disable
CLOCKOUT_PCIE_12	Disable	CLKREQ12	Disable
CLOCKOUT_PCIE_13	Disable	CLKREQ13	Disable
CLOCKOUT_PCIE_14	Disable	CLKREQ14	Disable
CLOCKOUT_PCIE_15	LAN	CLKREQ15	Disable
CLK_LPC0 (24MHz)	Disable		Disable
CLK_LPC1 (24MHz)	SIO	CLKRUN	Disable

PCH

Peripheral	IC
LAN	RTL8111H
VGA	IT6516BFN
SIO	IT8625E
TPM	NPCT650LAAYX (Header)
Function	Usage
ISH	Disable
CNVi	Disable
Deep Sx (DSW)	Disable
GSPI0/1/2	Disable
UART0/1/2	Disable
I2C0/1/2	Disable
SPI1	Disable
SD	Disable
INTRUDER	Enable

SIO

SIO	Index/Data	Clock
IT8625E	2E/2F	24MHz
Function	Usage	Action

COM1	enable	
COM2	enable	
LPT	enable	
KB	enable	
MS	enable	
3VSB	enable	enter S3 = enable, enter S5 = disable
5VSB_CTRL	enable	enter S5 = enable, exit S5= disable

Fan	Control by	Monitor by
CPU_FAN	FAN_CTRL1	CPU_TEMP
SYS_FAN	FAN_CTRL2	CPU_TEMP

Temp	Input port	Sense by
CPU_TEMP	PECI	
SYS_TEMP	TMPIN1	NTC

Voltage	Input port	Divider	Usage
VCORE	VIN0	Direct connect	H/W monitor
VDIMM	VIN1	Direct connect	H/W monitor
+12V	VIN2	10K/2K	PWRGD
+VCC	VIN3	15K/10K	H/W monitor
5VSB	VIN4	16.2K/8.87K	Use for 5VSB_SEN
+VCC3	VIN6	6.49K/10K	H/W monitor

GPIO	GPI/GPO	Usage	Action
GP22	GPO	FP_LED1	S0: H S3: L S4/S5: H
GP10	GPO	FP_LED2	S0: L S3: B S4/S5: H
GP47	GPI	GFX select	H:default BIOS L: onboard VGA

PCH GPIO

GPIO	GPI/GPO	Usage	Action
GPP_B11	GPO	ME disable	H: ME disable L: ME enable (default)
GPD2	GPI	COM_RI	L: Wakeup
GPP_A11	PME	SIO_PME	L: Wakeup
GPP_C16	GPO	patch KVM	DOS: H enter Win: L
GPP_F5	GP1	F_AUDIO Detect	H: AC97 L:HDA (reserved only)
GPP_C23	GPI	TPM IRQ	Reserved only
GPP_C18	GPI	BOM select	reserved
GPP_C20	GPI	BOM select	reserved
GPP_C22	GPI	BOM select	reserved

Flex I/O

Name	Usage	Combo Config	Topology	Length
USB1	USB3.0		Direct Connect	7.6"
USB2	USB3.0		Direct Connect	7.3"
USB3	USB3.0		Cable Connect	3.2"
USB4	USB3.0		Cable Connect	3.3"
USB5	X			
USB6	X			
PCIE1/USB7	X			
PCIE2/USB8	X			
PCIE3/USB9	X			
PCIE4/USB10	X			
PCIE5	LAN		Direct Connect	5.8"
PCIE6	PCIEX1		Direct Connect	4.1"
PCIE7	PCIEX1		Direct Connect	4.5"
PCIE8	PCI BRIDGE		Direct Connect	3.6"
PCIE9/SATA0	X			
PCIE10/SATA1	X			
PCIE11	M.2 SSD 2 lanes		M.2	2.6"
PCIE12	M.2 SSD 2 lanes		M.2	2.5"
PCIE13/SATA0	SATA1	SATA	Cable Connect	3.2"
PCIE14/SATA1	SATA2	SATA	Cable Connect	2.7"
PCIE15/SATA2	SATA3	SATA	Cable Connect	3.4"
PCIE16/SATA3	SATA4	SATA	Cable Connect	3.0"
PCIE17/SATA4	X			
PCIE18/SATA5	X			
PCIE19	X			
PCIE20	X			
PCIE21	X			
PCIE22	X			
PCIE23	X			
PCIE24	X			

USB2.0

Name	Location	Topology	Length
USB1	FUSB1	Internal Cable	3.0"
USB2	FUSB1	Internal Cable	3.0"
USB3	USB3F	Internal Cable	4.0"
USB4	USBLAN	Back Panel	6.4"
USB5	USB3R	Back Panel	7.5"
USB6	USBLAN	Back Panel	6.6"
USB7	USB3R	Back Panel	7.5"
USB8	FUSB2	Internal Cable	3.0"
USB9	USB3F	Internal Cable	4.2"
USB10	FUSB2	Internal Cable	3.0"
USB11	X		
USB12	X		
USB13	X		
USB14	X		



Elitegroup Computer Systems

Title			BIOS Configuration		
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